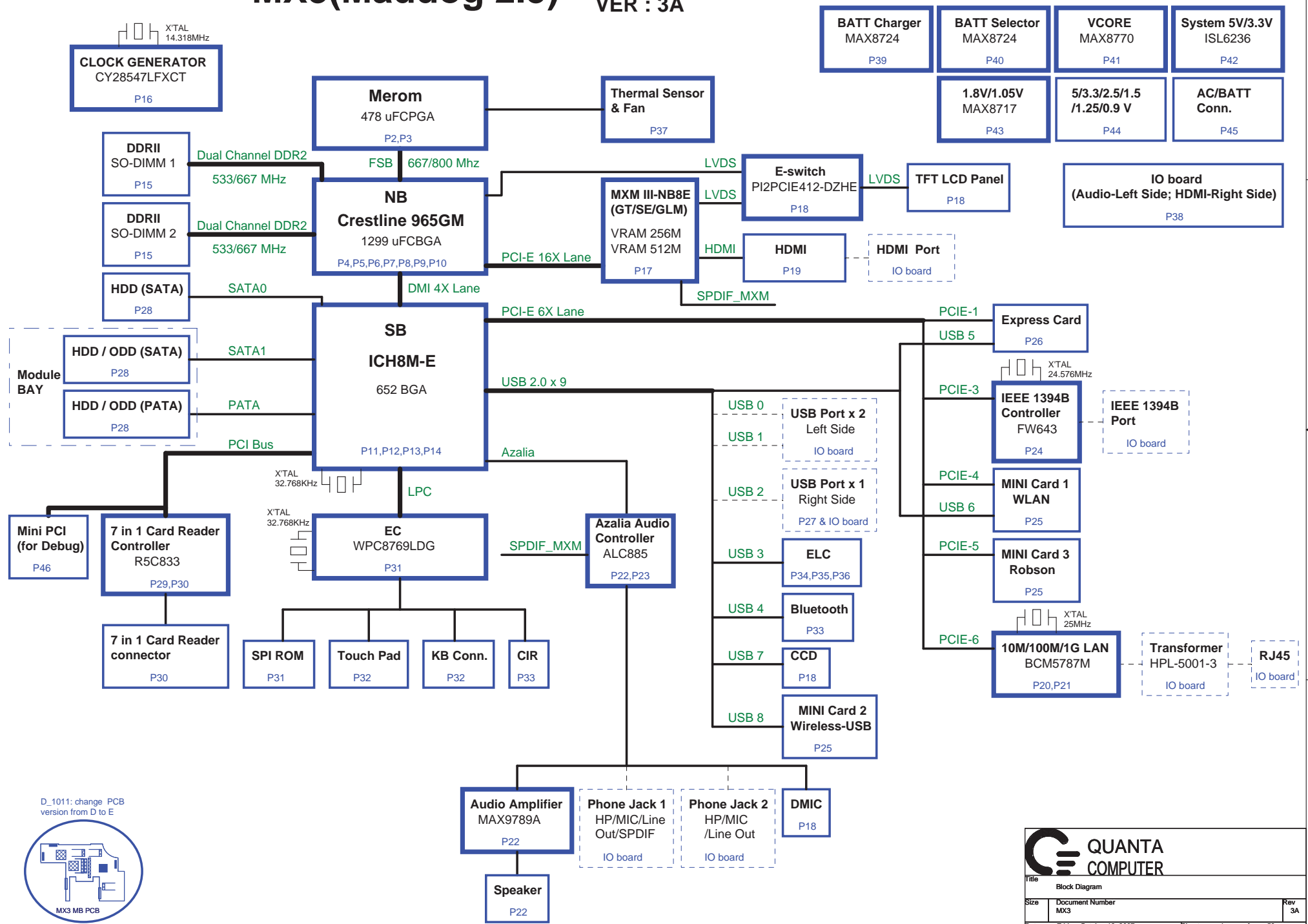
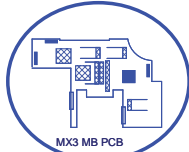



MX3(Maddog 2.5) VER : 3A



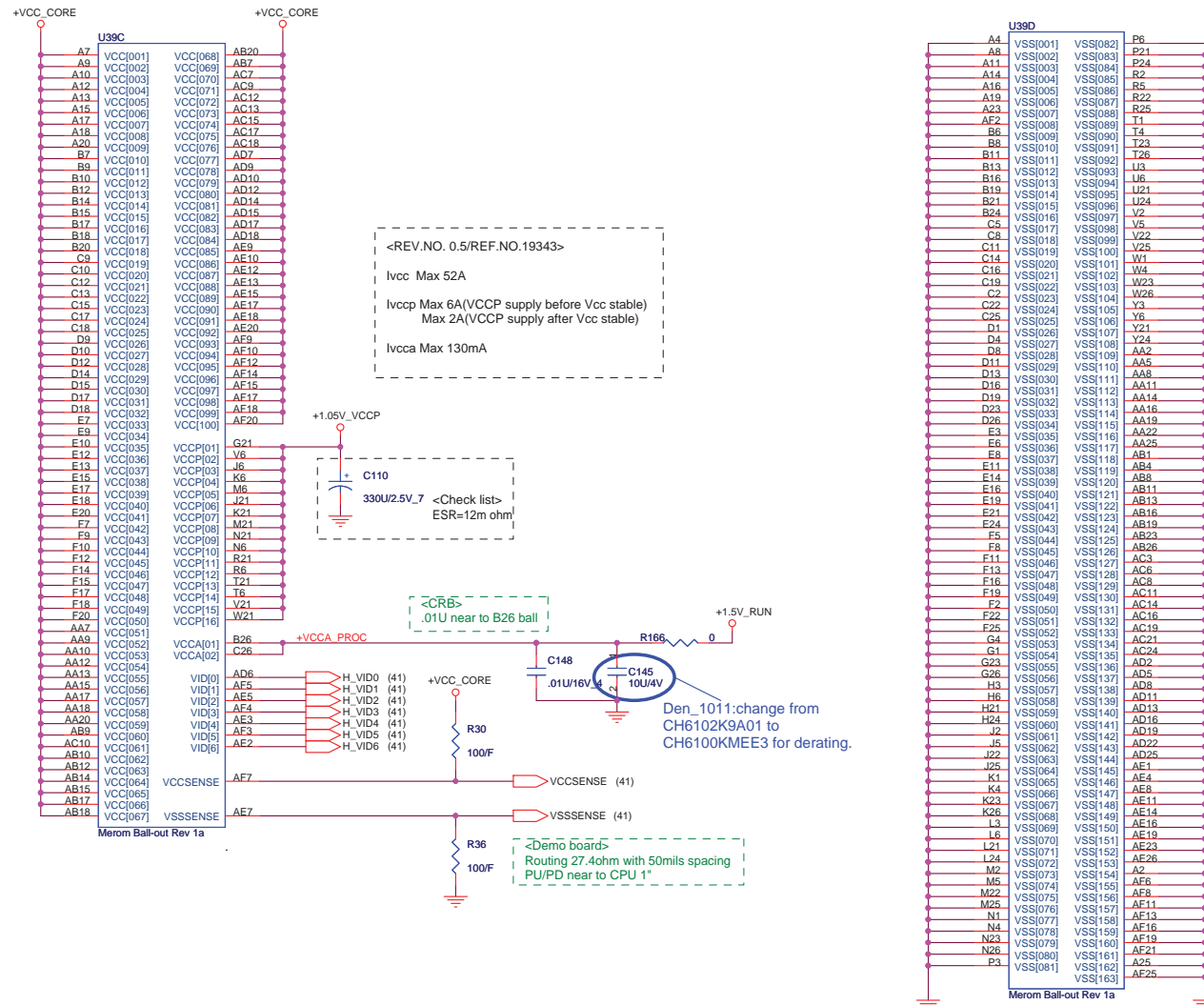
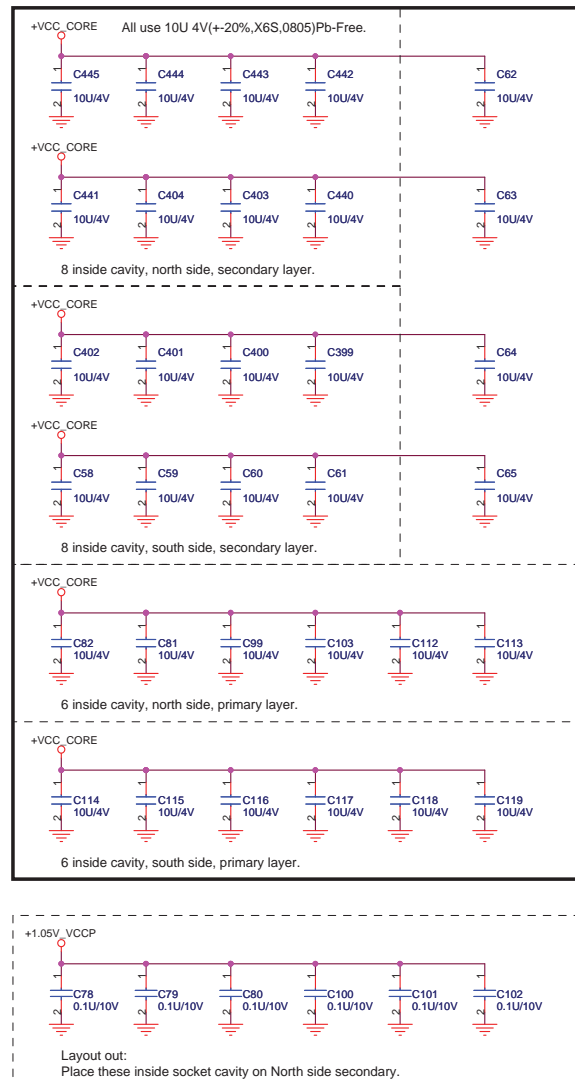
D_1011: change PCB version from D to E

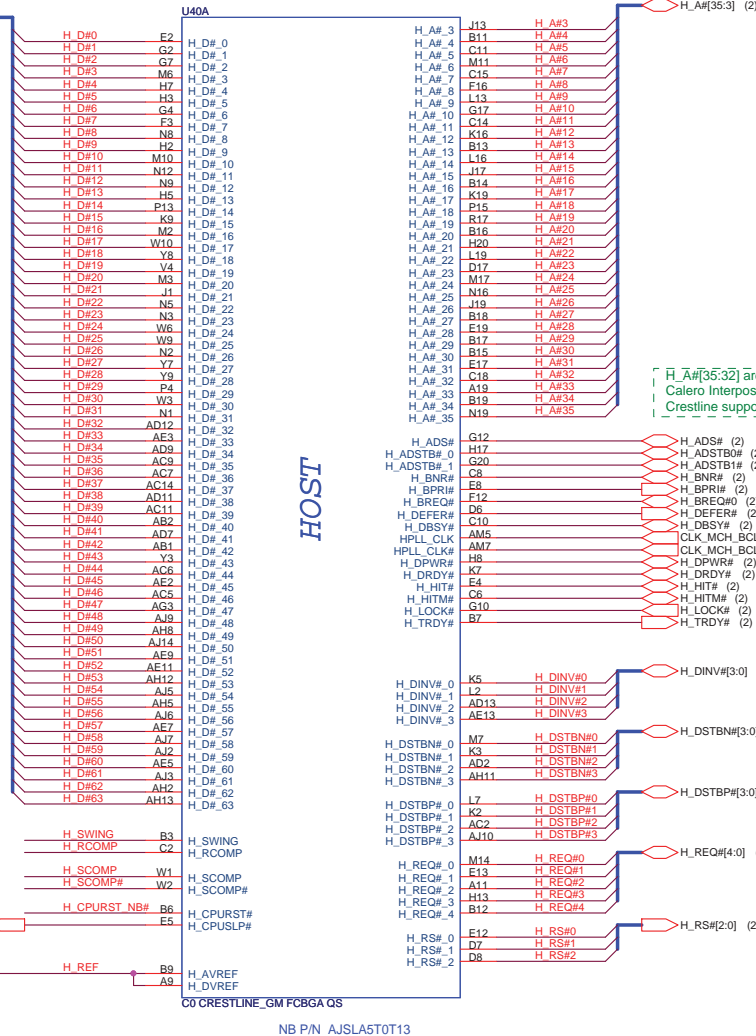
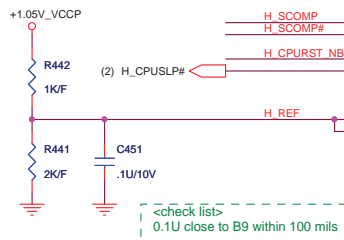
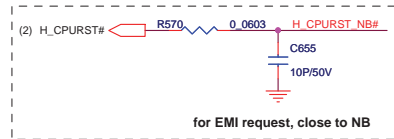
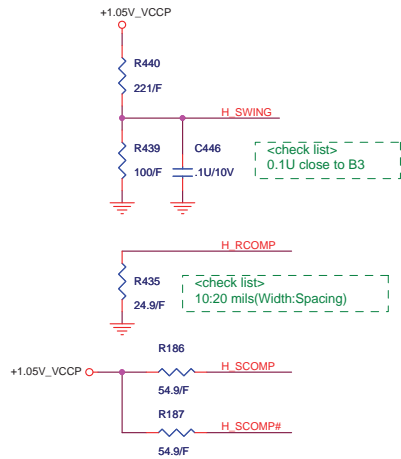


Title			
Block Diagram			
Size	Document Number	Rev	
MX3	MX3	3A	
Date:	Friday, October 12, 2007	Sheet	1 of 53

 QUANTA COMPUTER	
Title: CPU Host(1/2)	
Size: Document Number MX3	Rev 2A
Date: Friday, October 12, 2007	Sheet 2 of 53

CPU(Power)





H_A# [35:32] are not supported in
 Calero Interposer
 Crestline support 36 bit address



Strapping table

All strap are sampled with respect to the leading edge of the GMCH power ok signal

CFG[17:3] have internal pull-up

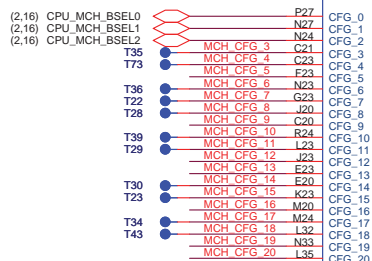
CFG[18:19] have internal pull-down

Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Reserved 01 = ALL-Z Mode Enabled 10 = XOR Mode Enabled 11 = Clock Gating Enabled (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIe x1 is operation (Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

INTEL CRB
ADD 0.1UF

U40B



NB(Memory controller)

DDR SYSTEM MEMORY A

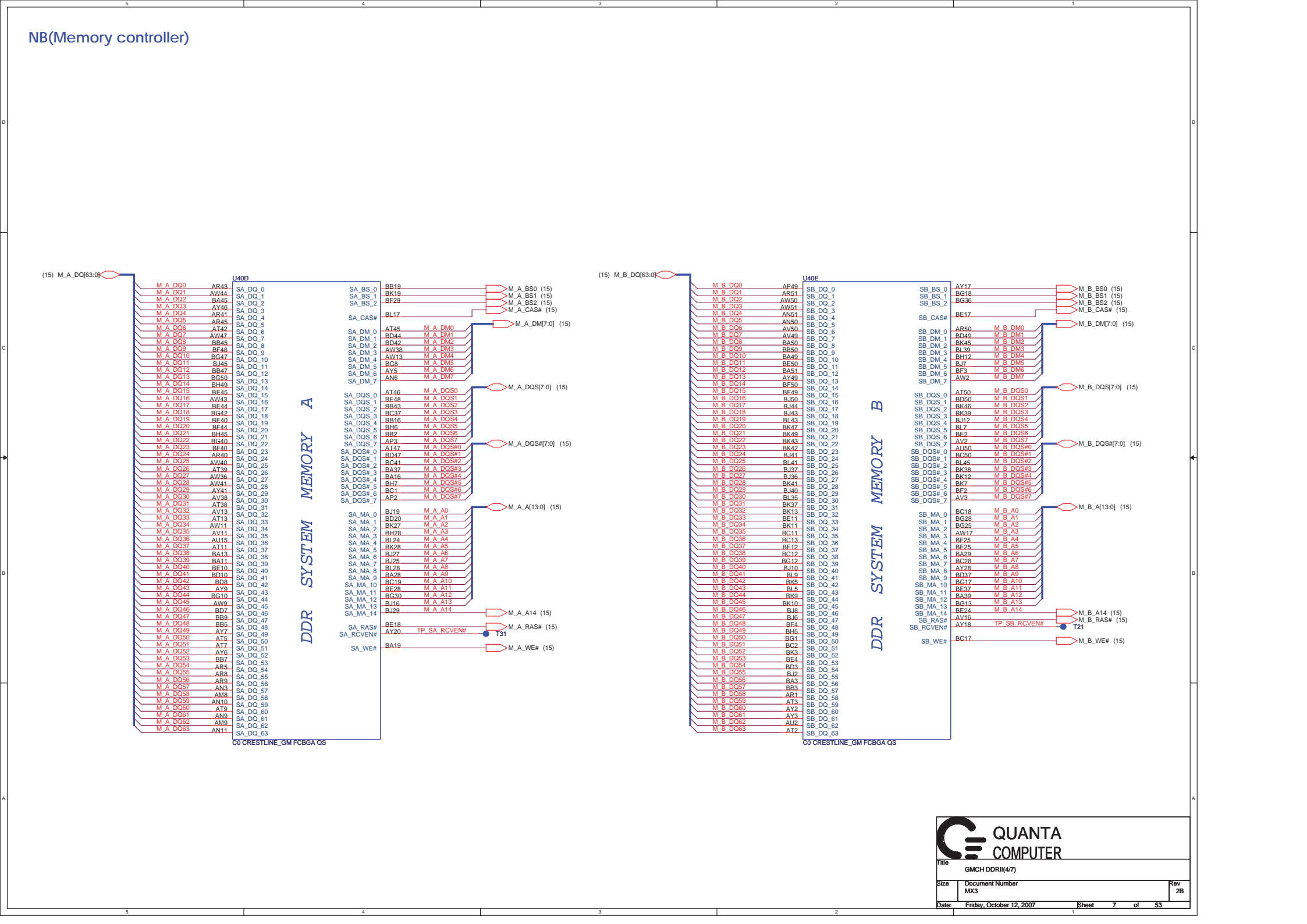
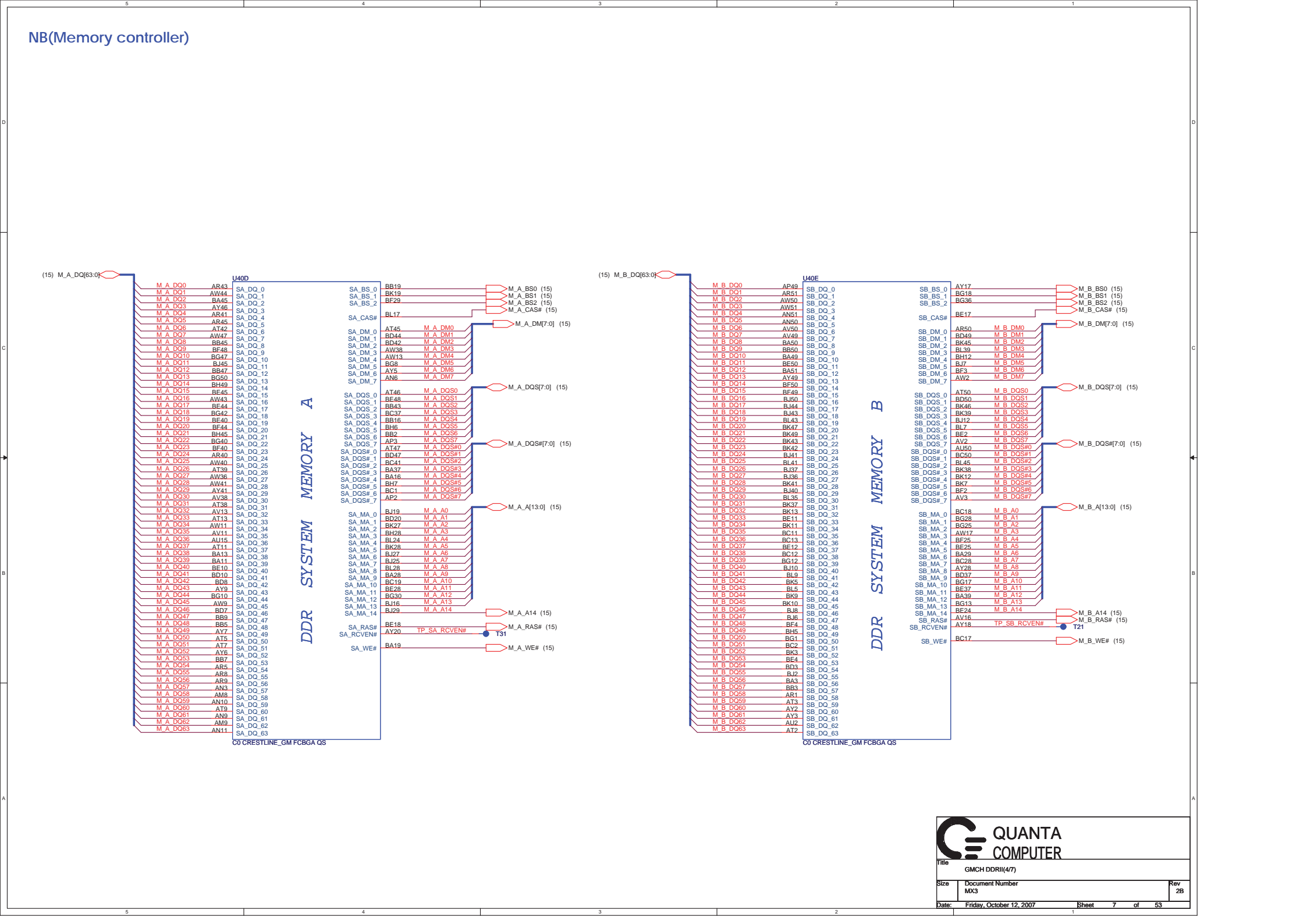
DDR SYSTEM MEMORY B

QUANTA COMPUTER

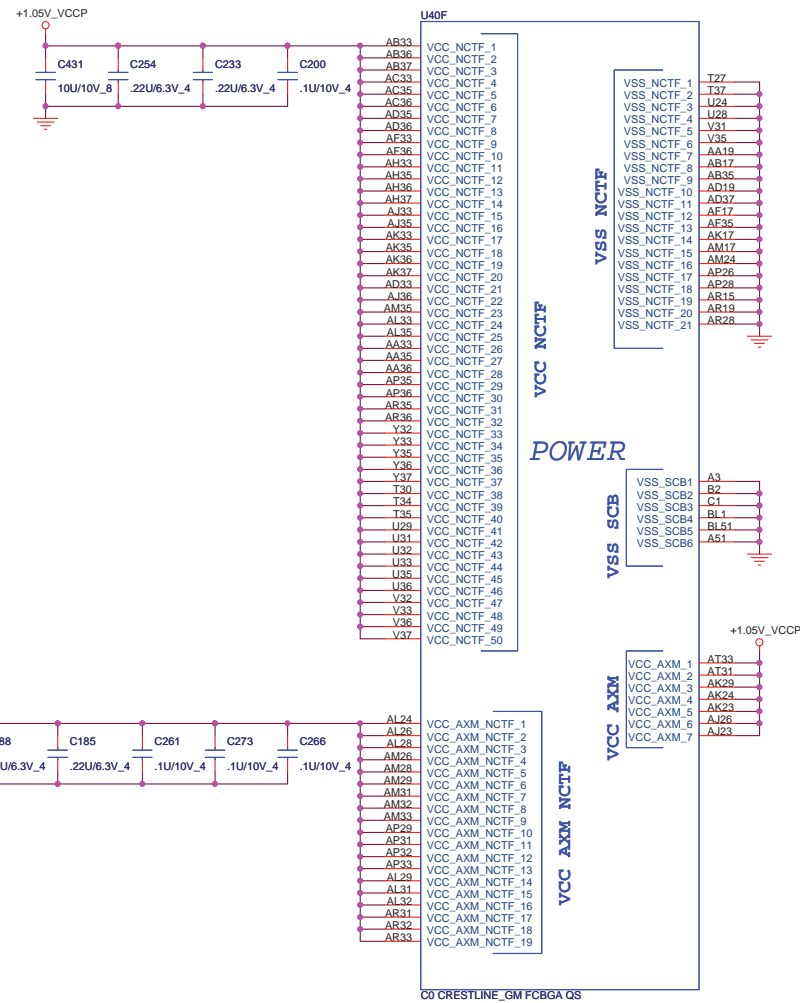
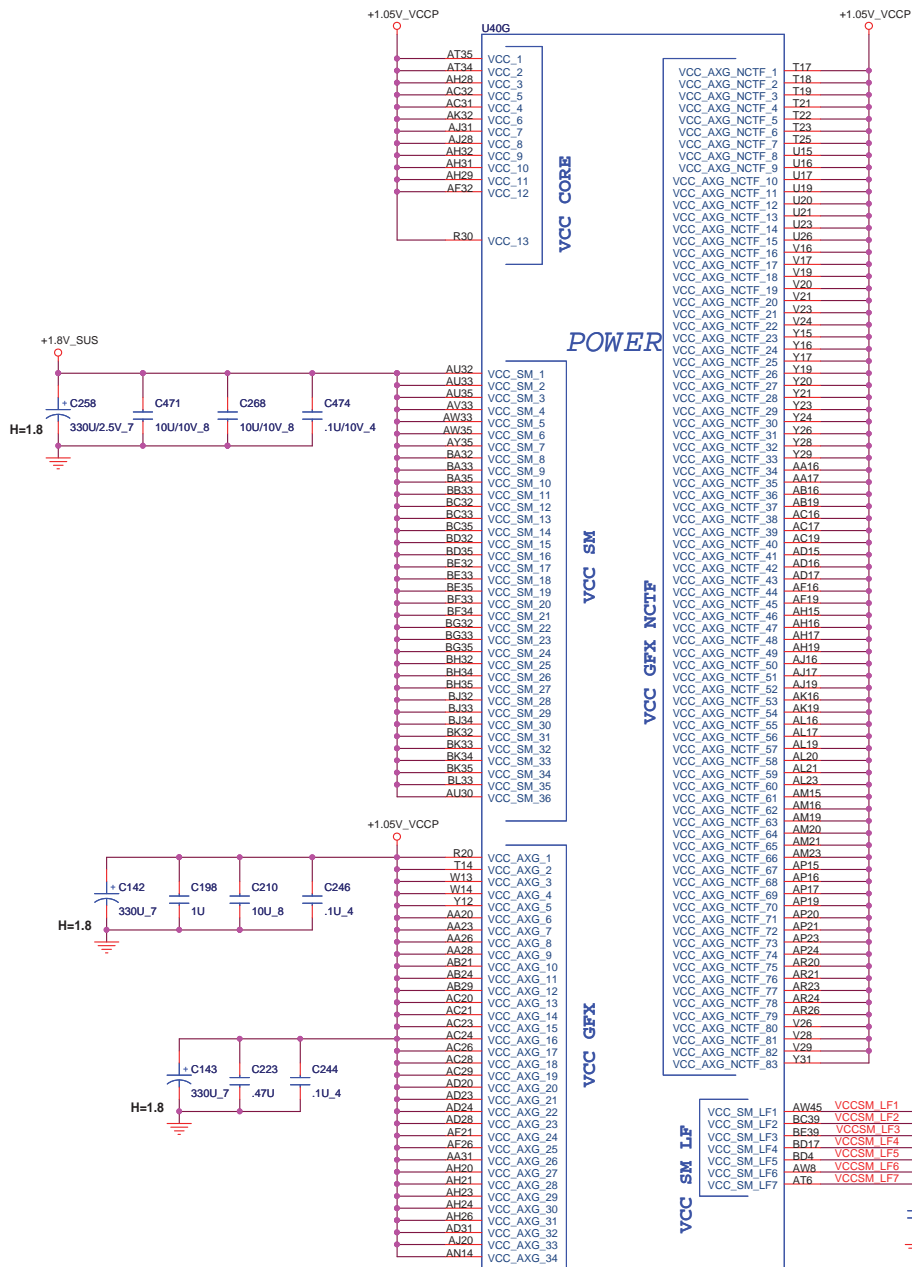
GMCH DDRIII(4/7)

Size Document Number **Rev**
MX3 2B

Date: Friday, October 12, 2007 **Sheet** 7 **of** 53



NB(Power-1)

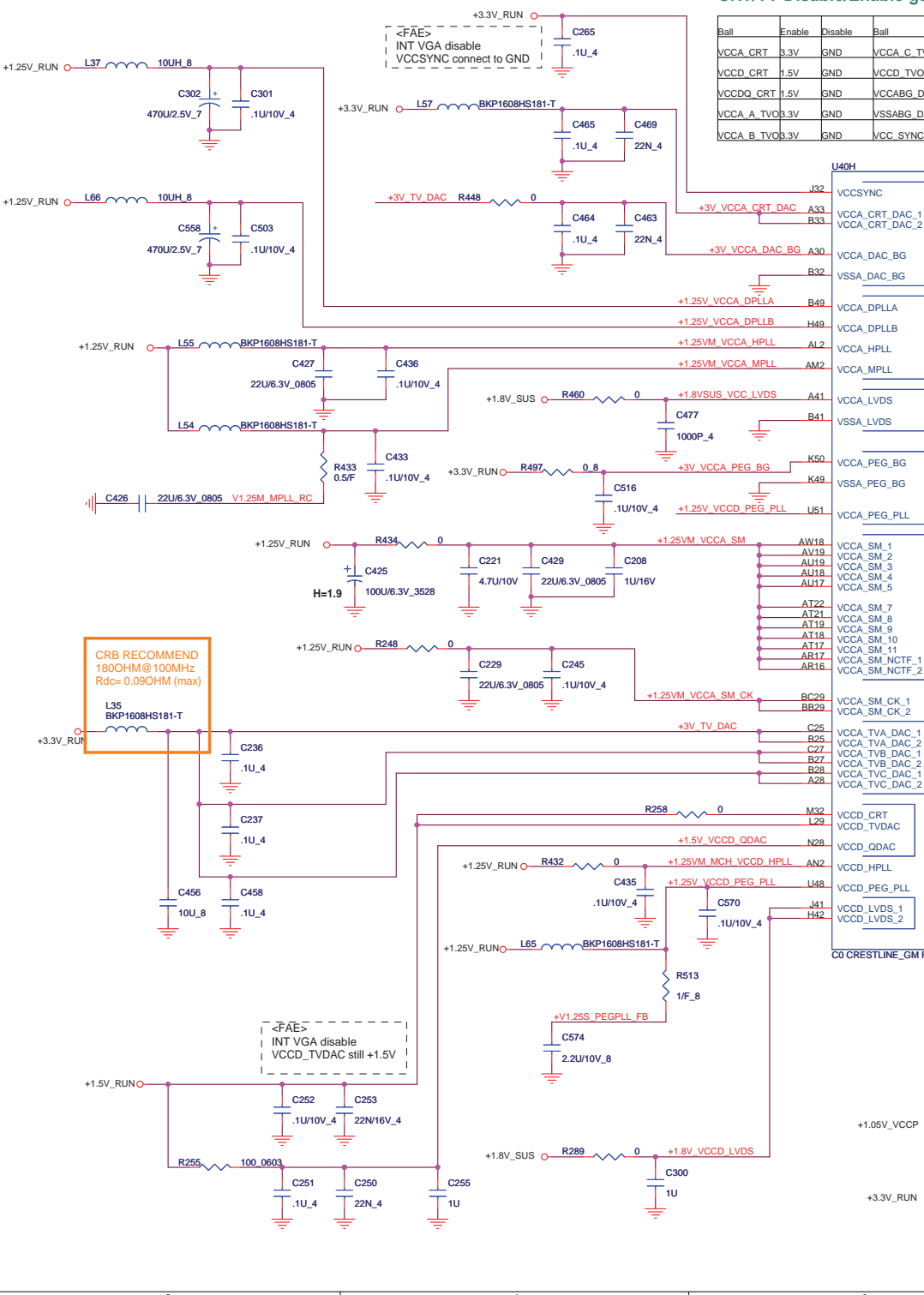


QUANTA
COMPUTER

Title GMCH Power-1(5/7)

Size	Document Number MX3	Rev 21
Date:	Friday, October 12, 2007	Sheet 8 of 53

NB(Power-2)




CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TV03.3V	GND	GND	VSSABG_DAC	GND	GND
VCCA_B_TV03.3V	GND	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

POWER

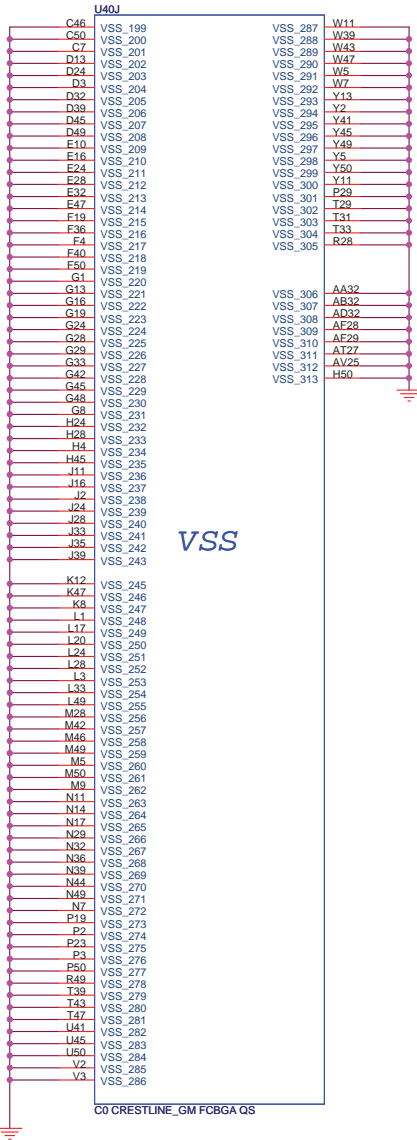
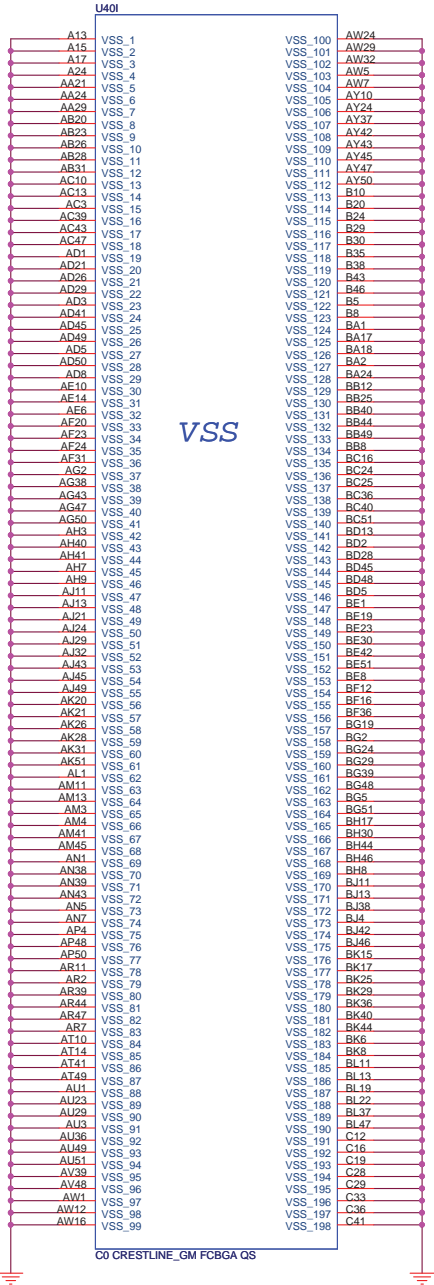


**QUANTA
COMPUTER**

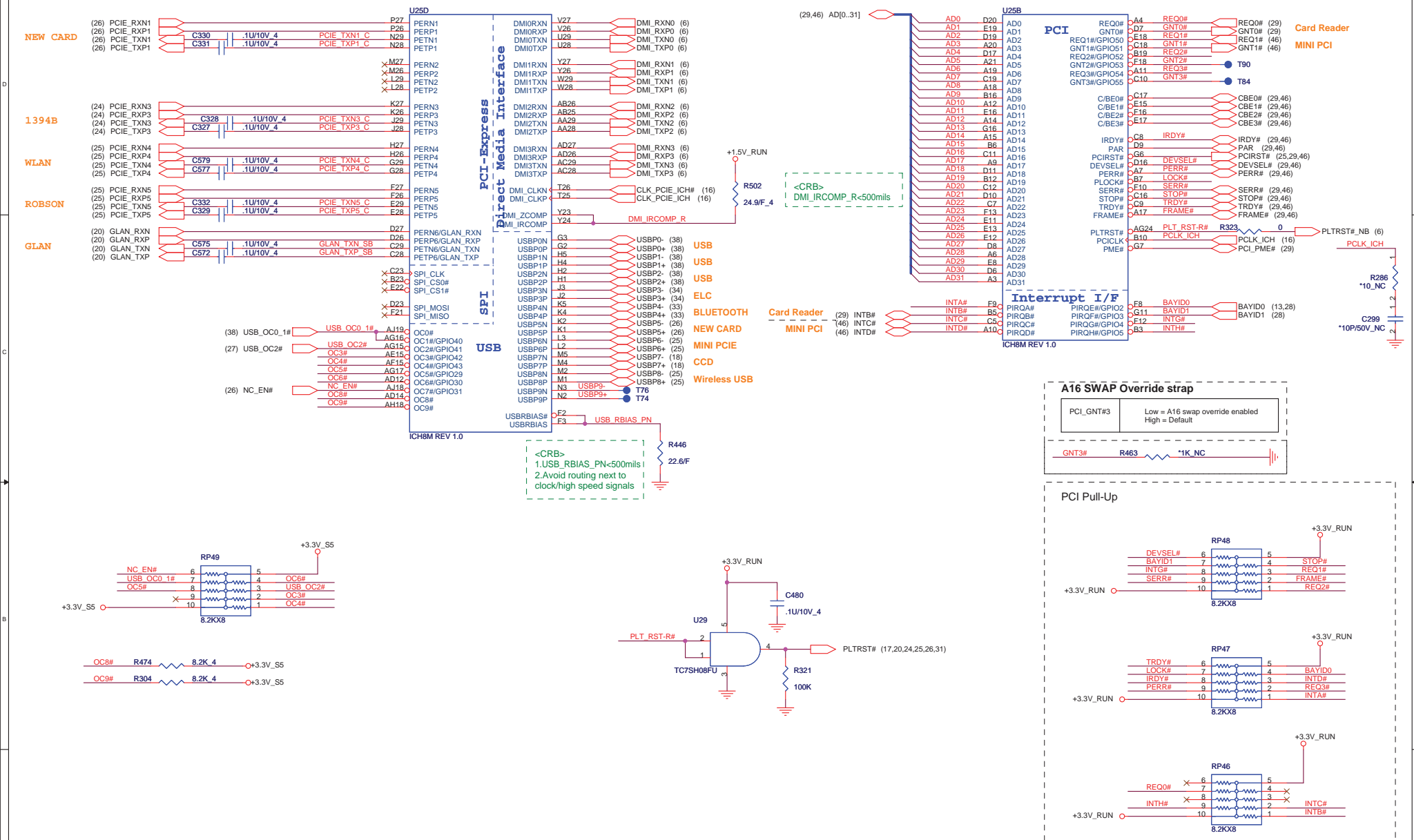
Title: GMCH Power-2(6/7)

Size: MX3	Document Number: MX3	Rev: 2B
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Date: Friday, October 12, 2007 Sheet 9 of 53



SB-PCI



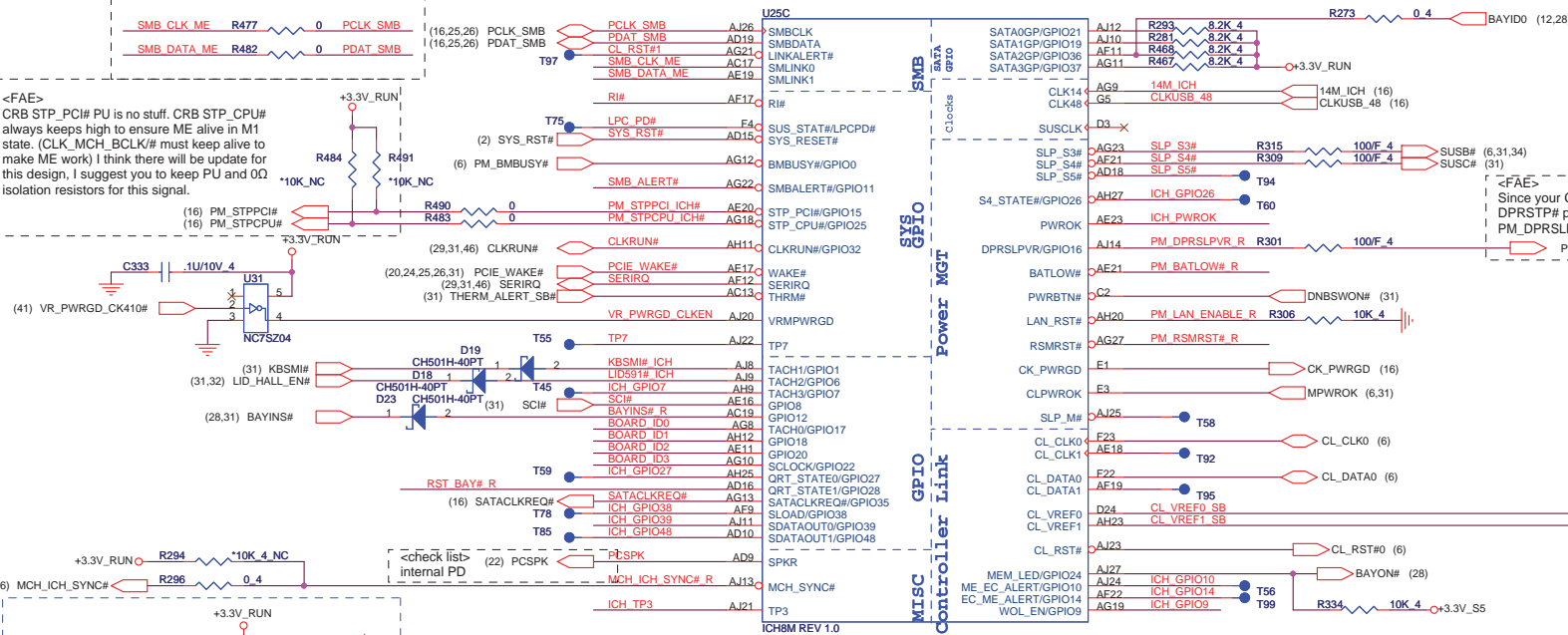
Title ICH8M PCIE/PCI/USB(2/4)

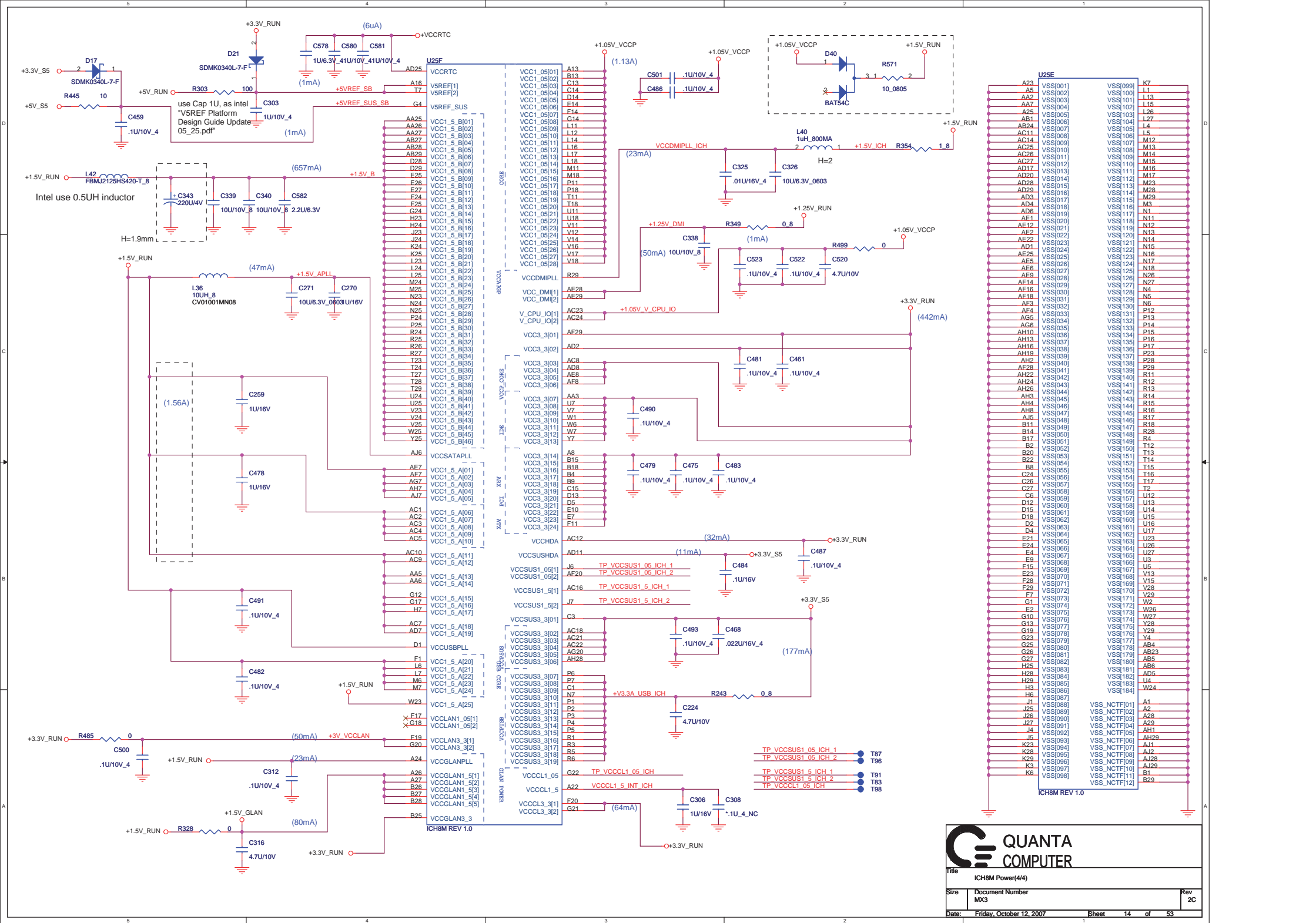
Size	Document Number MX3
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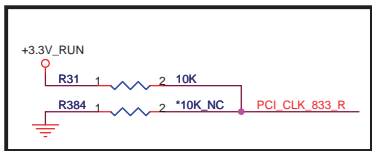
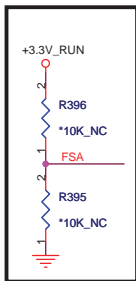
Date: Friday, October 12, 2007

Rev
2B

As Intel's review (Apr.,17,2007), add 0 ohm between SMBus & SMLINK to let SMBus of ICH8M work in slave mode.





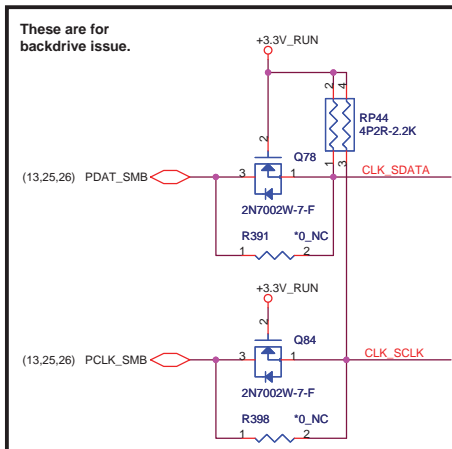
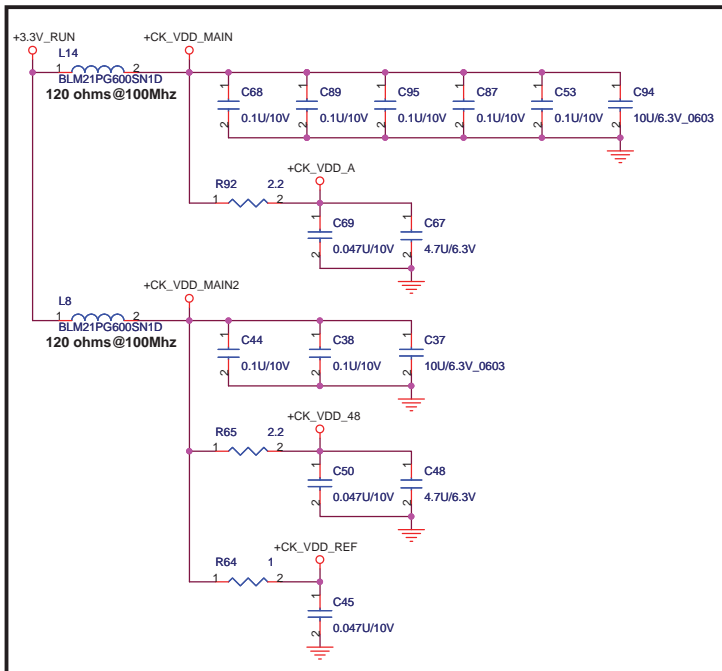
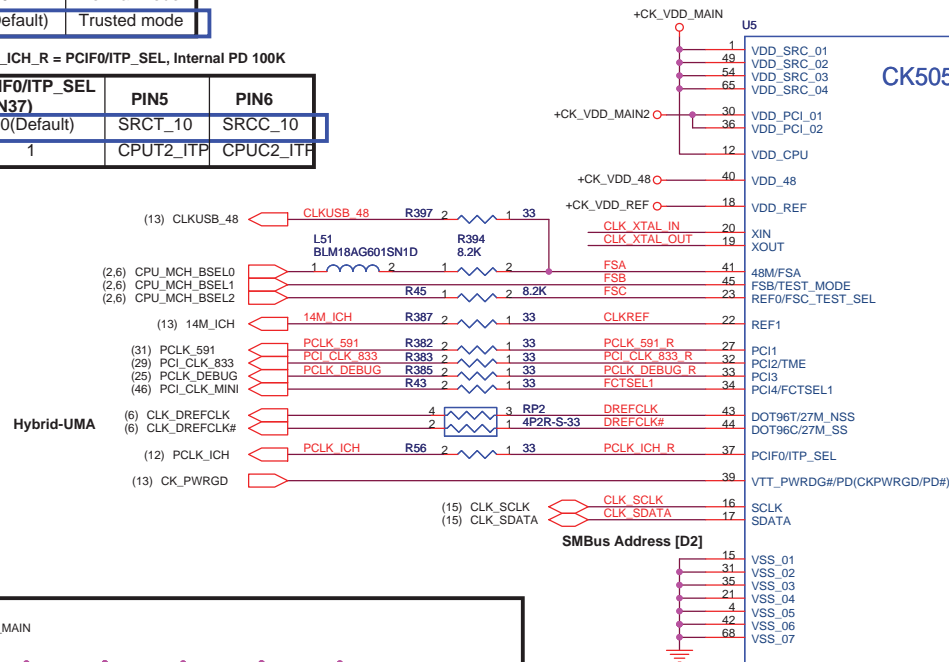
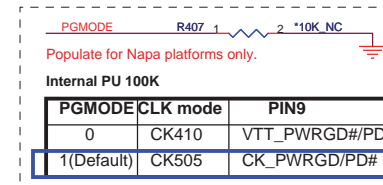
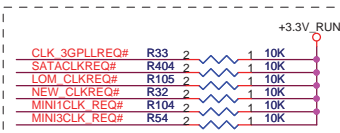
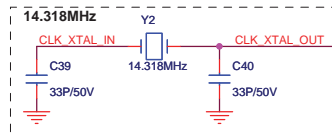
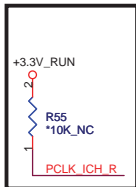


PCI_CLK_833_R = PCI2/TME, Internal PU 100K

PCI2/TME	PIN32
0	Normal mode
1(Default)	Trusted mode

PCLK_ICH_R = PCIF0/ITP_SEL, Internal PD 100K

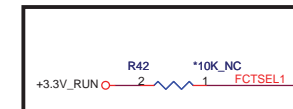
PCIF0/ITP_SEL (PIN37)	PIN5	PIN6
0(Default)	SRCT_10	SRCC_10
1	CPUT2_ITP	CPUC2_ITP

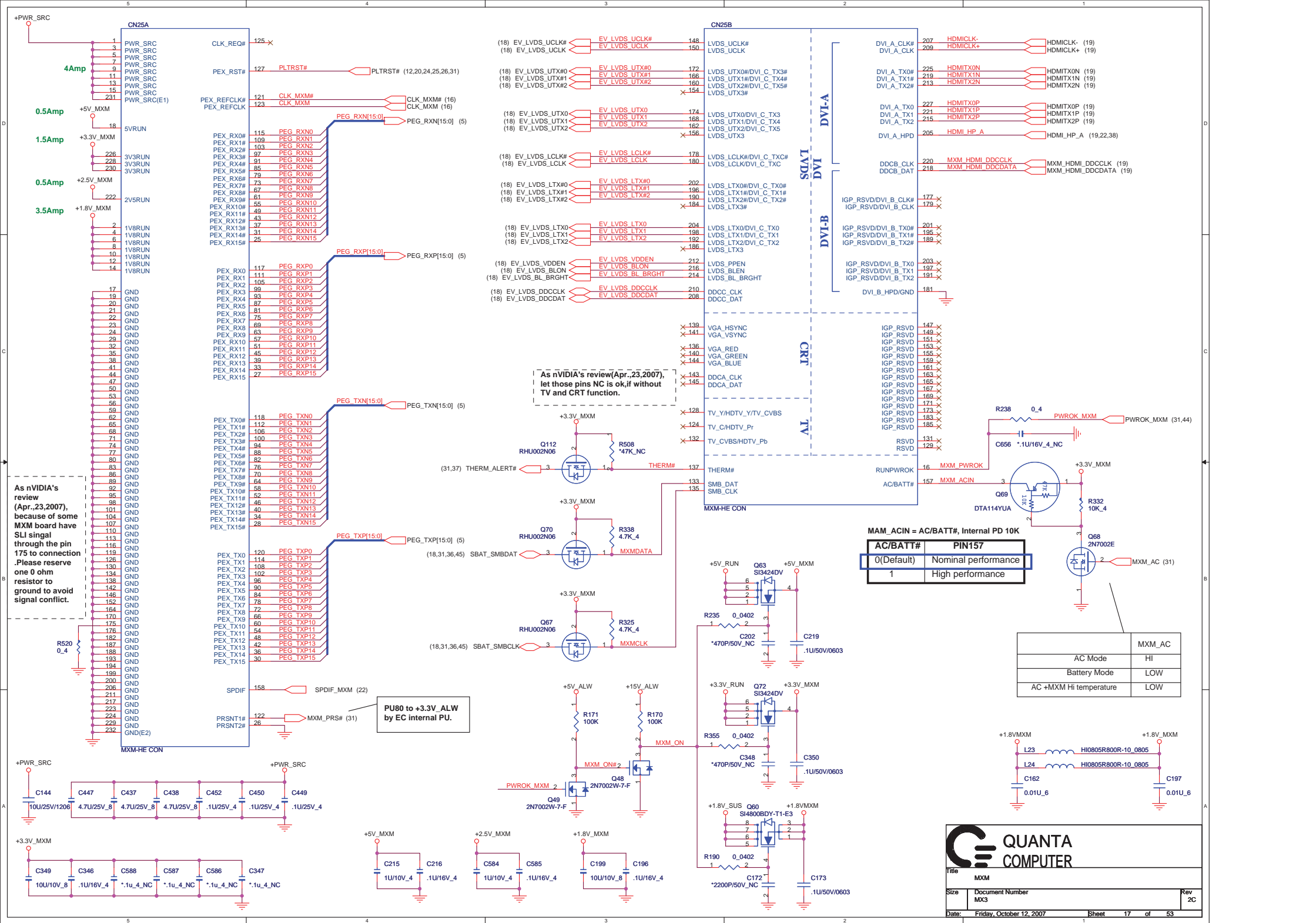


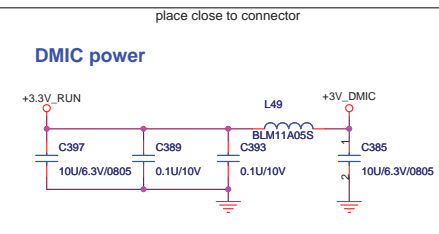
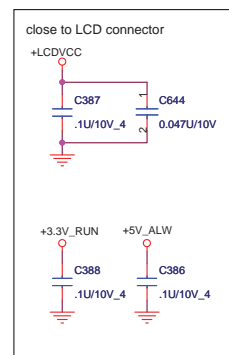
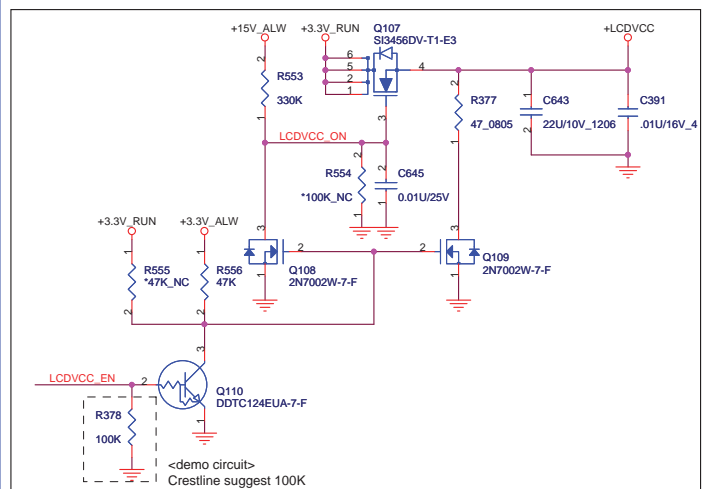
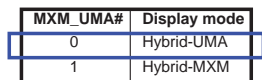
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

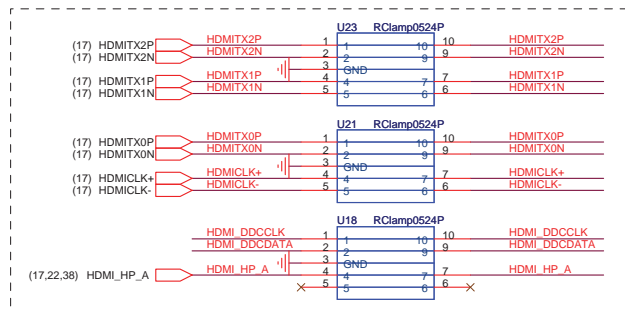
FCTSEL1 = PC4/FCTSEL1, Internal PD 100K

PC4/FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Discrete	27M_NSS	27M_SS	SRCT0	SRCC0

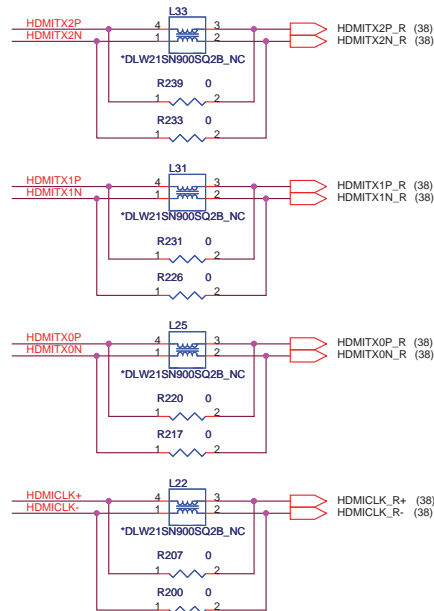
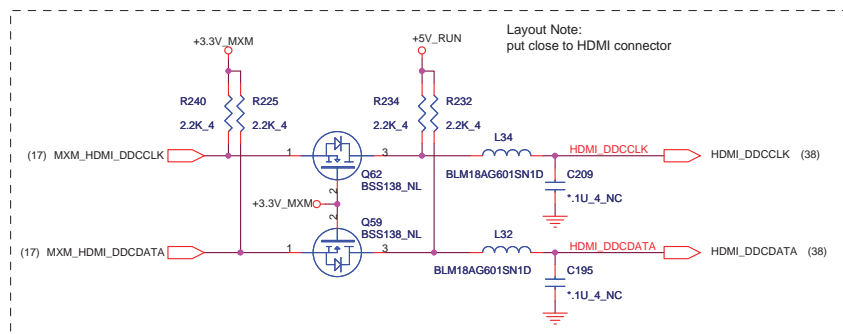






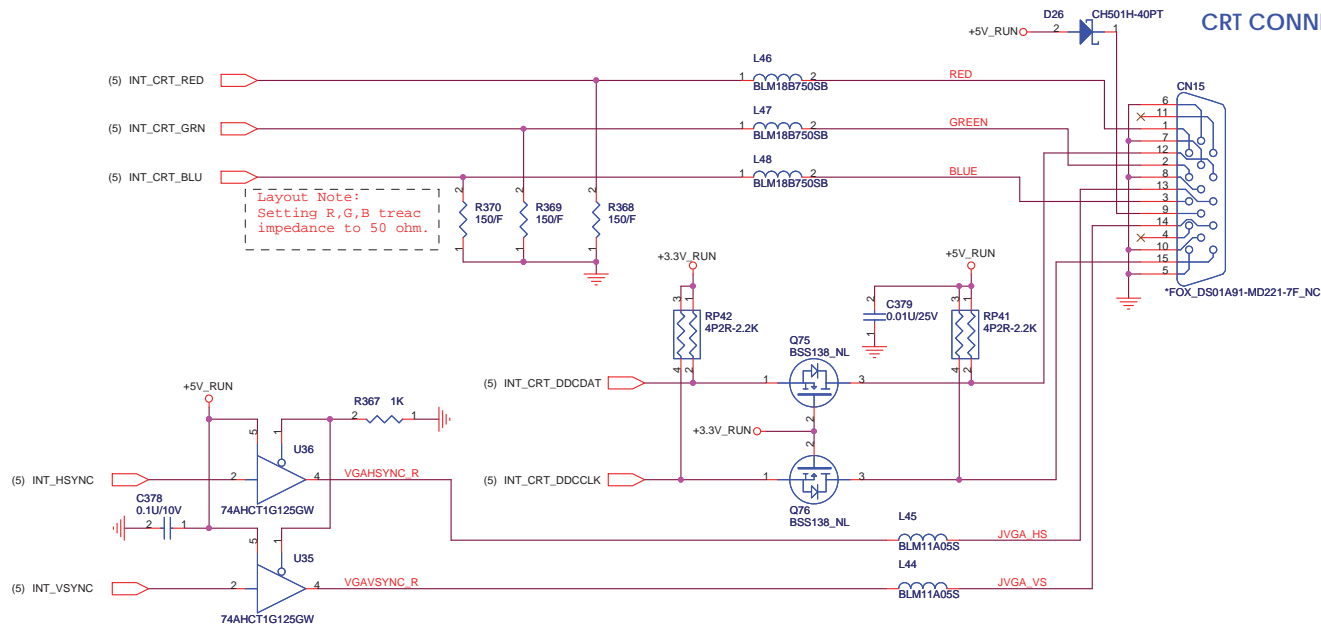


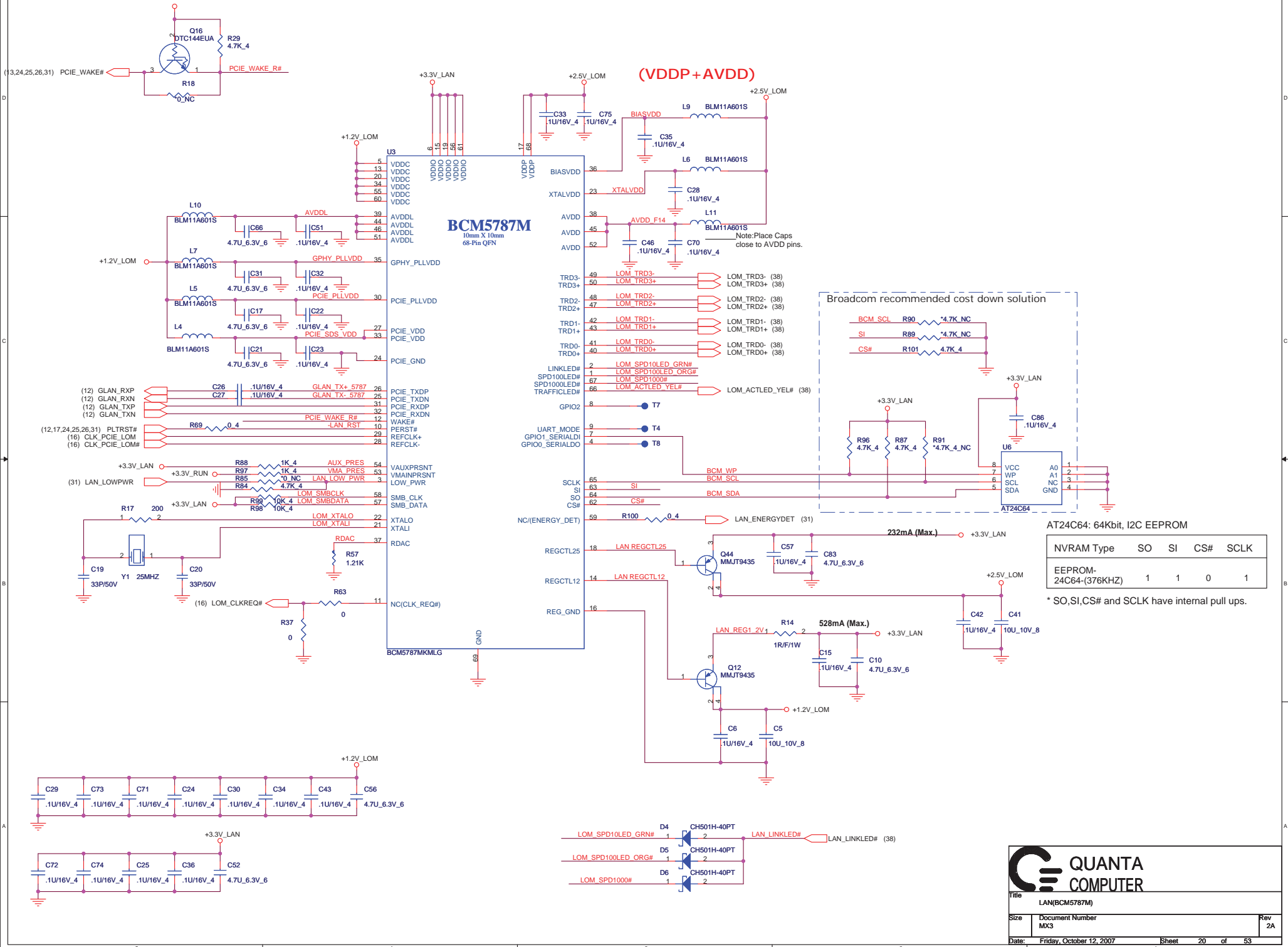
for ESD




for EMI

CRT CONNECTOR FOR Debug







QUANTA
COMPUTER

Title

LAN(BCM5787M)

Size

Document Number

MX3

Rev

2A

Date:

Friday, October 12, 2007

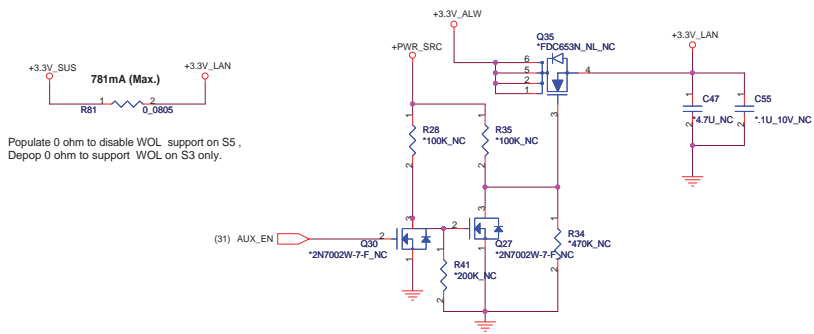
Sheet

20

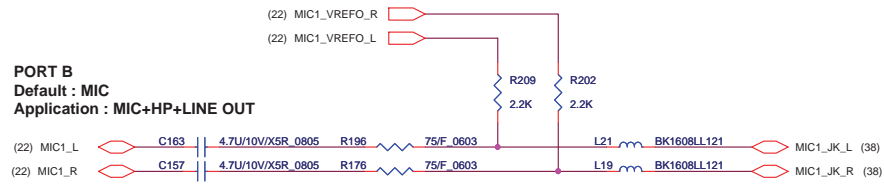
of

53

LAN POWER

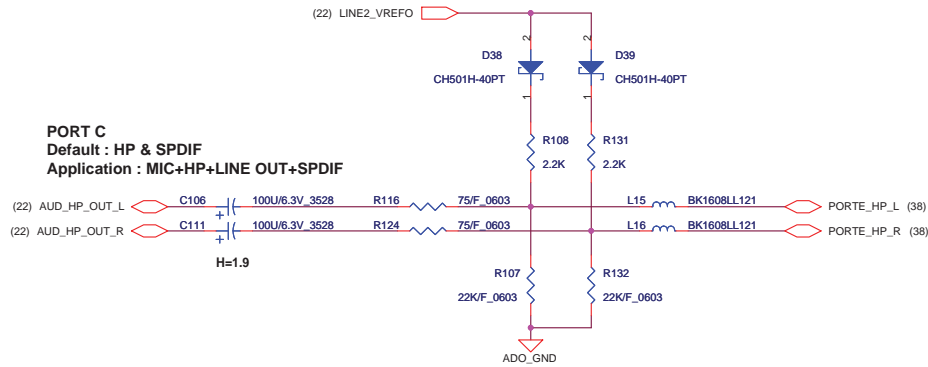


PORT B
Default : MIC
Application : MIC+HP+LINE OUT

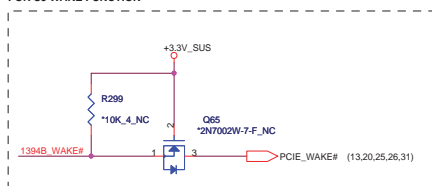


1. In order to meet Vista Premium requirements, MLCC input cap must use X5R dielectric material and 10V DC rated voltage.
2. If use polarity 100uF cap, then need to add 22K pull-down resistors.
3. R196, R176, R116, R124 are used for enhancing Audio quality and ESD ability.

PORT C
Default : HP & SPDIF
Application : MIC+HP+LINE OUT+SPDIF



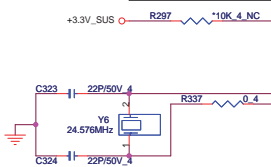
FOR S3 WAKE FUNCTION



(12,17,20,25,26,31) PLTRST#

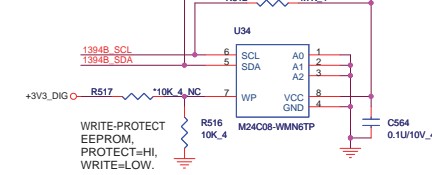
(16) CLK_PCIE_1394B
(16) CLK_PCIE_1394B#
(12) PCIE_TXP3
(12) PCIE_TXN3
(12) PCIE_RXP3
(12) PCIE_RXN3

FOR S3 WAKE FUNCTION

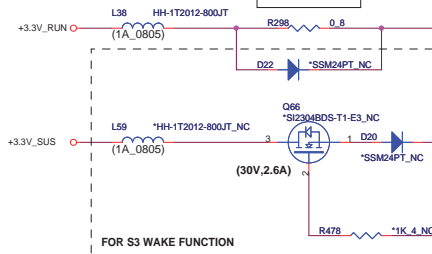


For FW643 rev03, EEPROM is not supported for code reading, pop this Res. For rev04, EEPROM is supported, depop this Res. Considering the cost saving, may pop this Res always for code reading from BIOS.

EEPROM FUNCTION



IF SUPPORT S3 WAKE FUNCTION, DEPOPULATE THE RESISTOR.



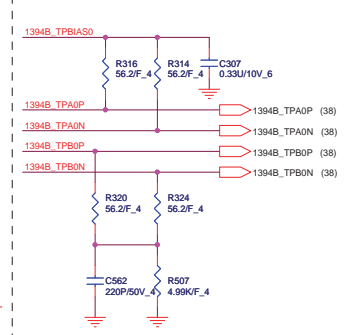
FOR S3 WAKE FUNCTION

AGERE FW643

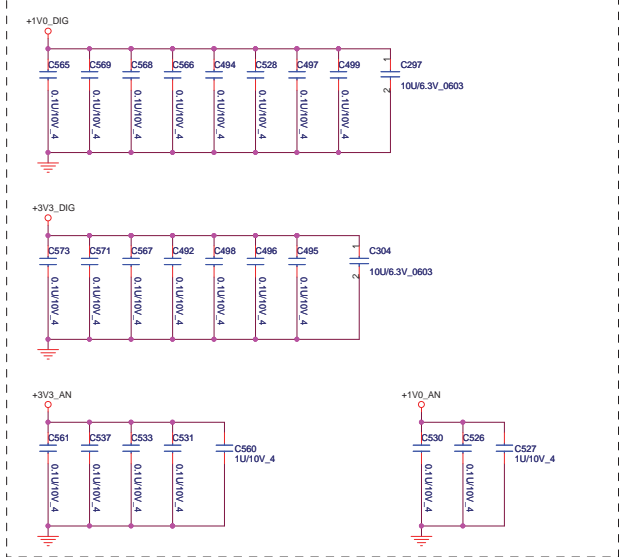
0.8mm BALL PITCH

Agere 1394b(PCIE)_FW643_11X11

CLOSE TO CHIP within 500 mil



CLOSE TO PER POWER PIN

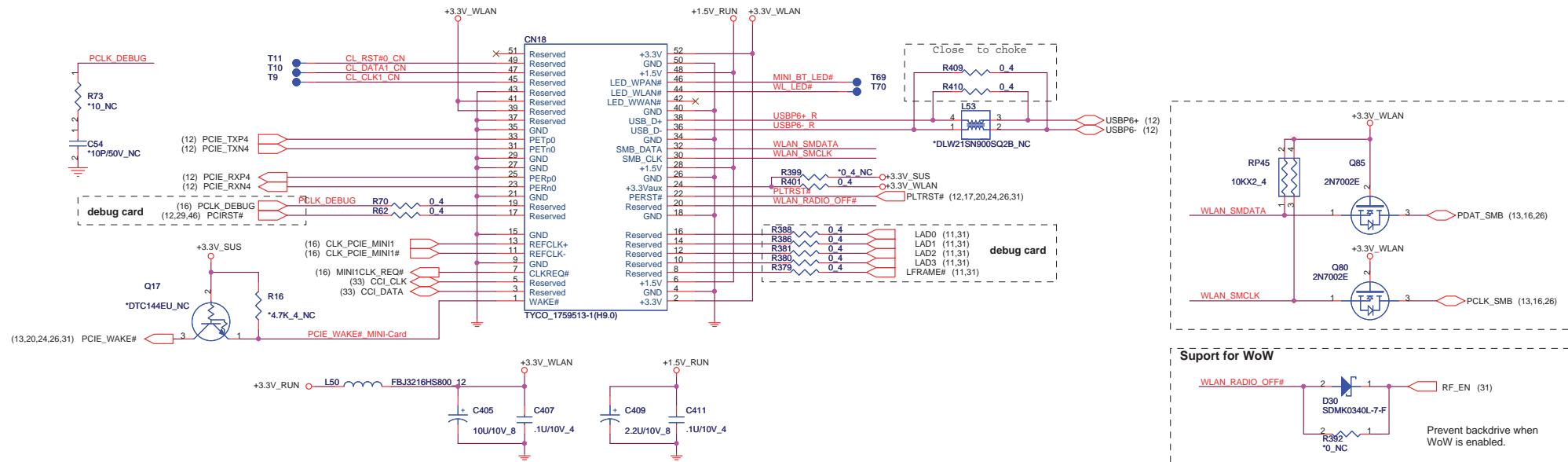


Note: Collector Pins on Transistor to be connected to CAPs using large heatsink 0.4 sq in on Top Side

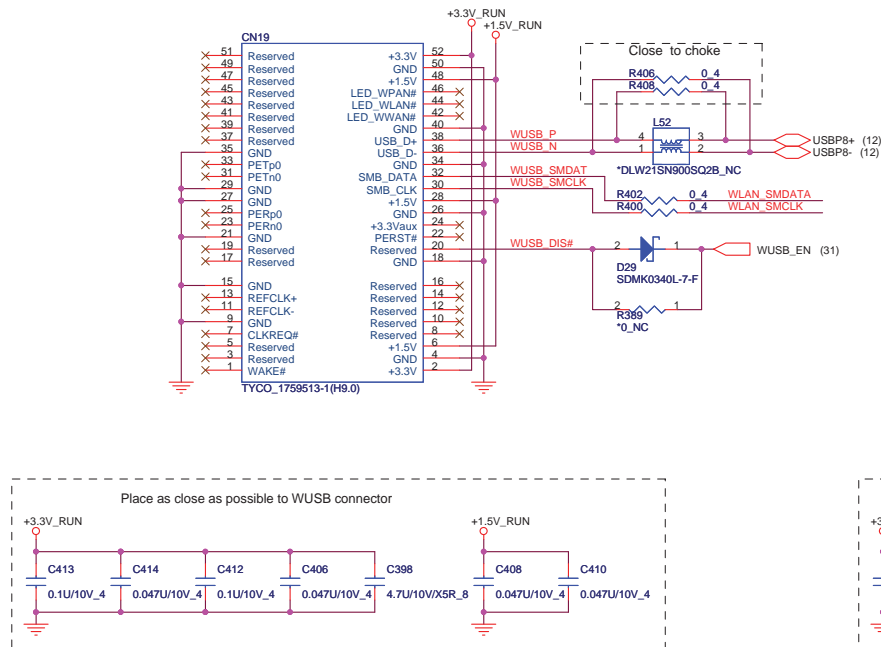
Multiple Vias to DND



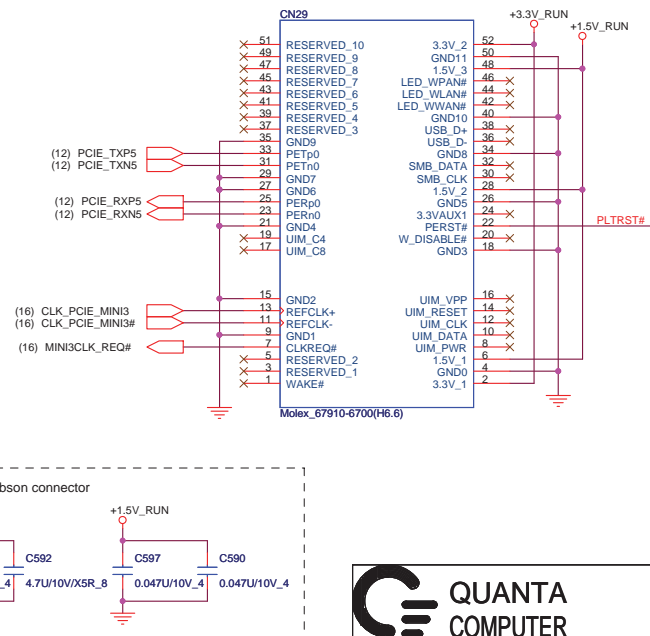
MiniCard connector - WLAN



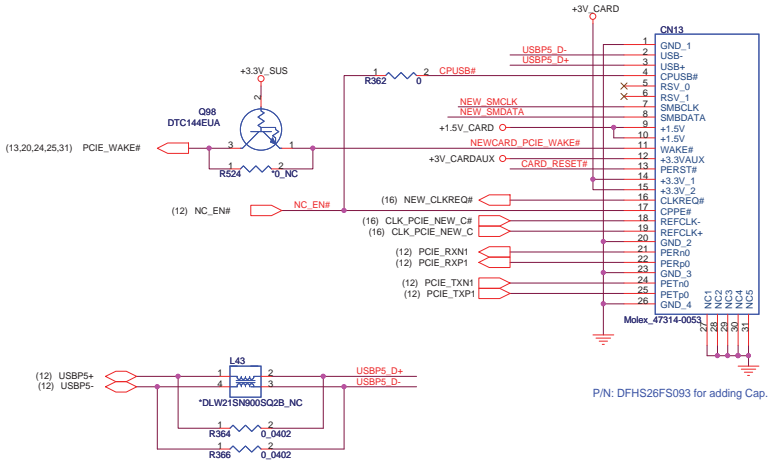
MiniCard connector - Wireless-USB



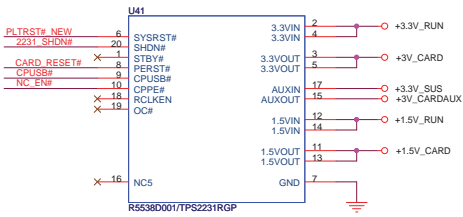
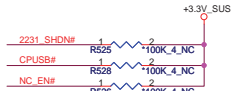
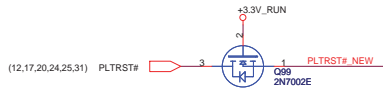
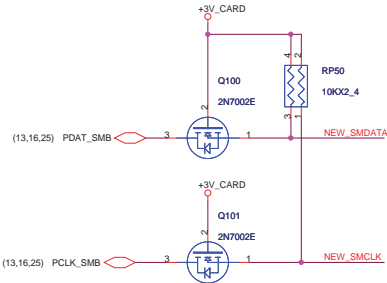
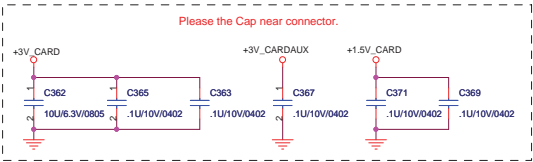
MiniCard connector - Robson



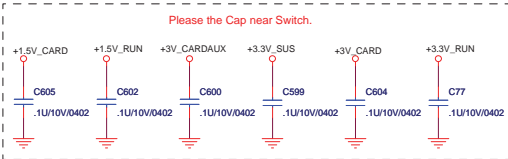
Express Card



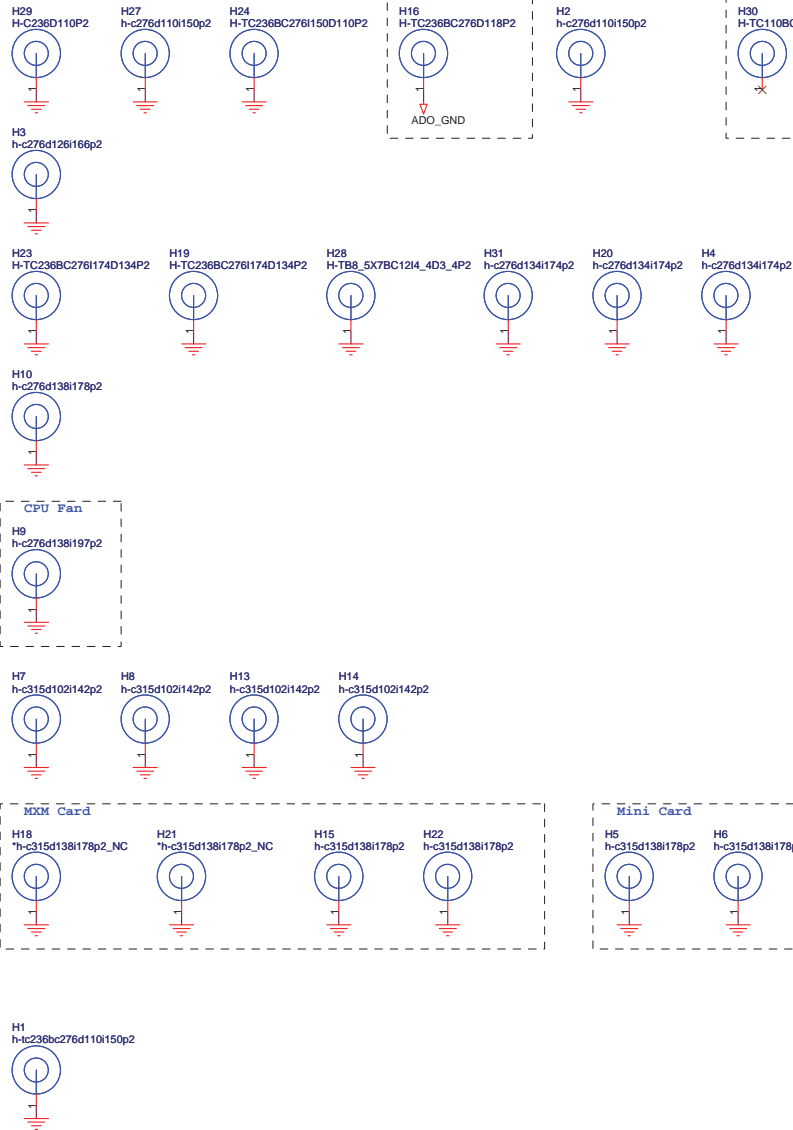
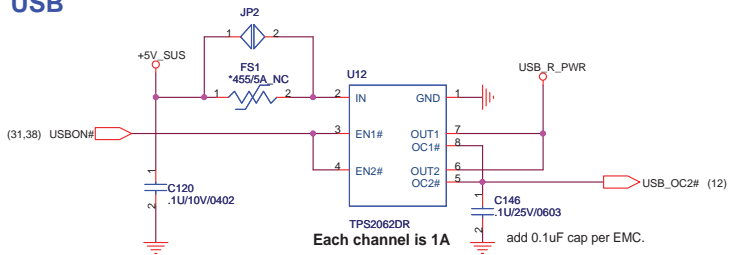
P/N: DFHS26FS093 for adding Cap.



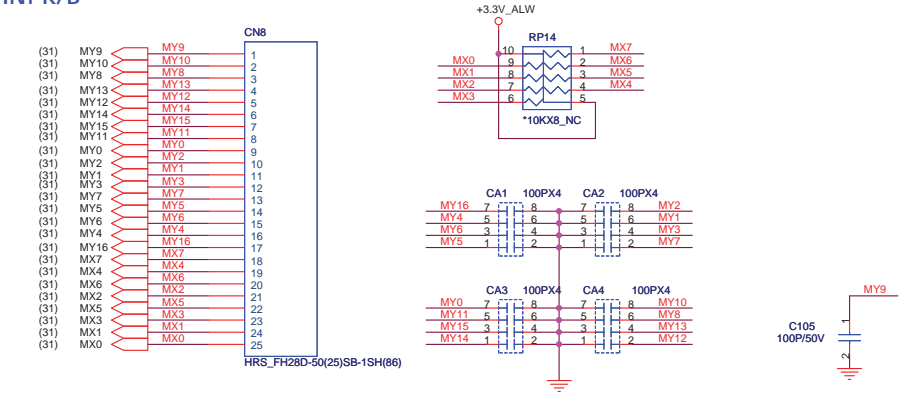
+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA
+3V_CARDAUX Max. 400mA, Average 275mA



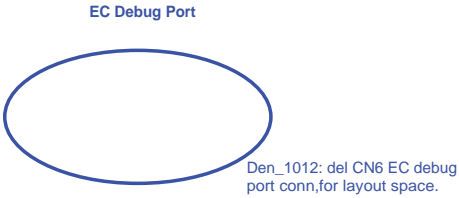
USB



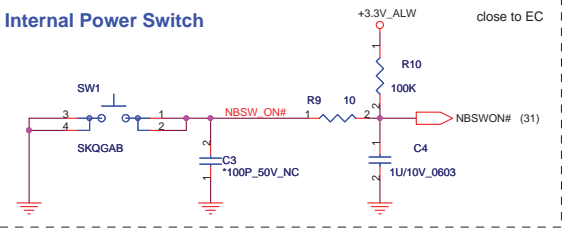
INT K/B



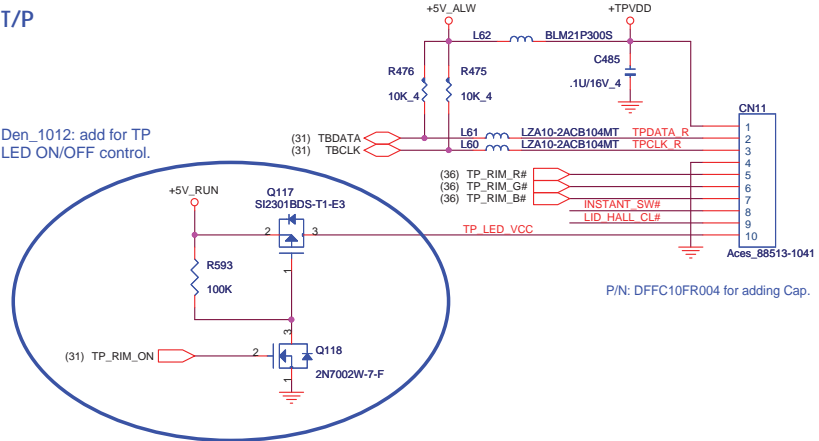
DEBUG PORT



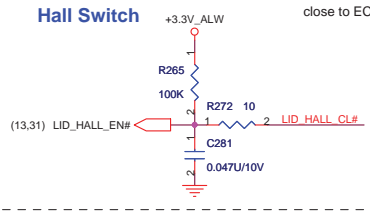
Internal Power Switch



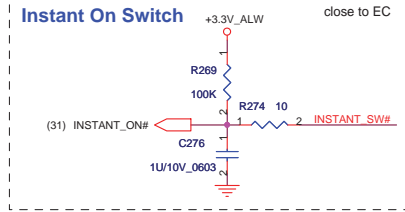
T/P



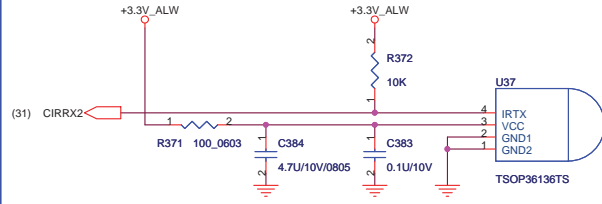
Hall Switch



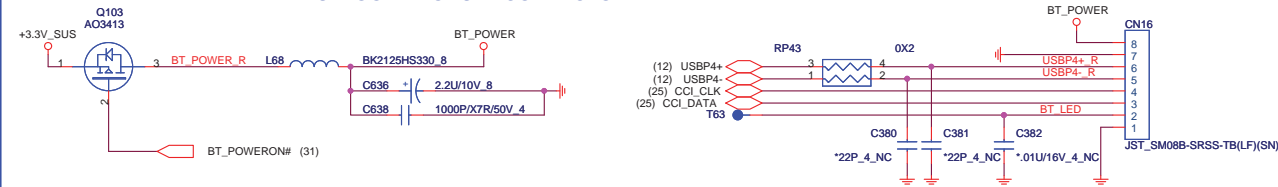
Instant On Switch



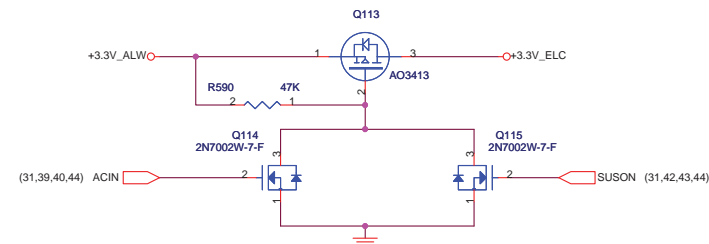
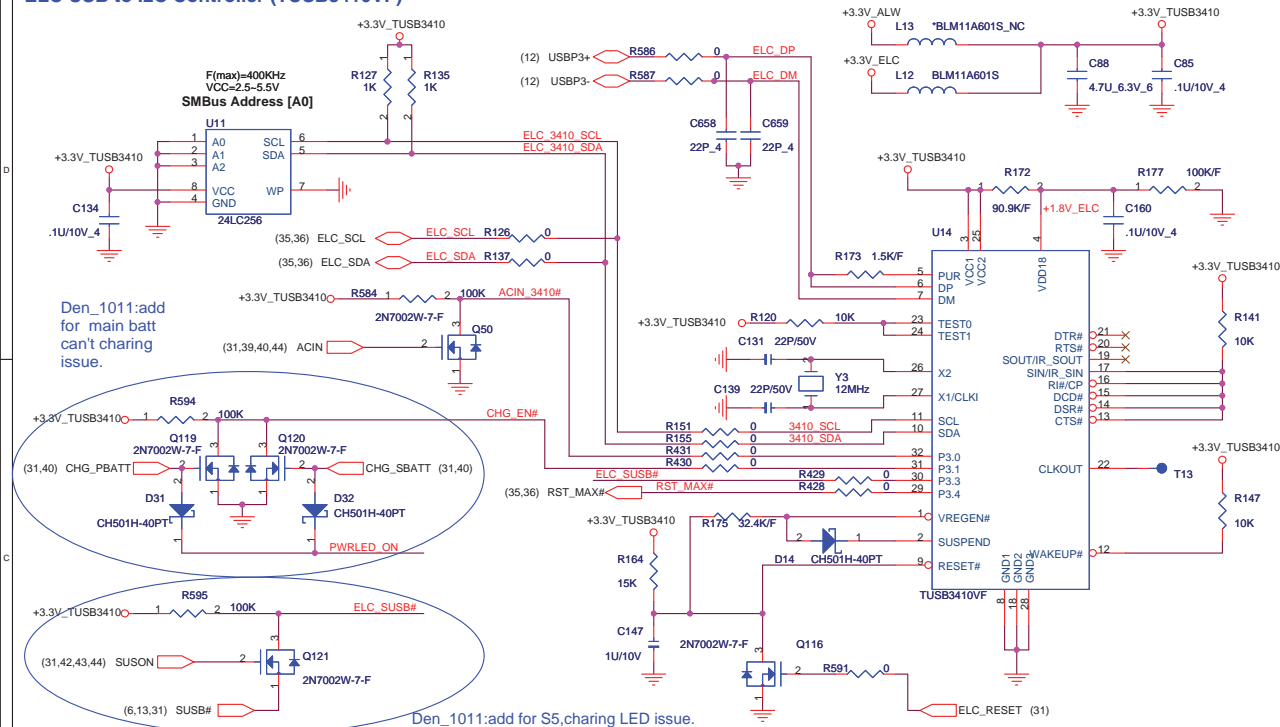
CIR module



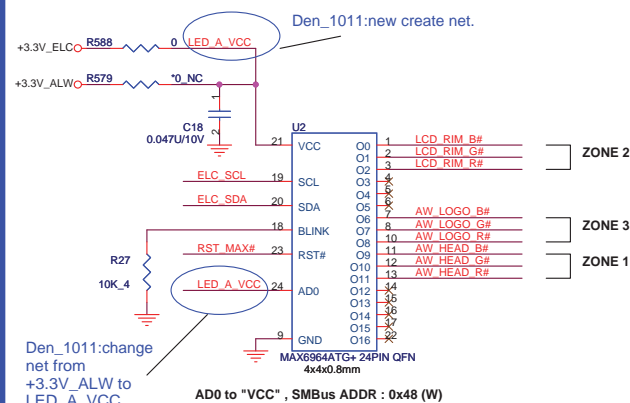
BLUETOOTH MODULE CONNECTOR



ELC USB to I2C Controller (TUSB3410VF)

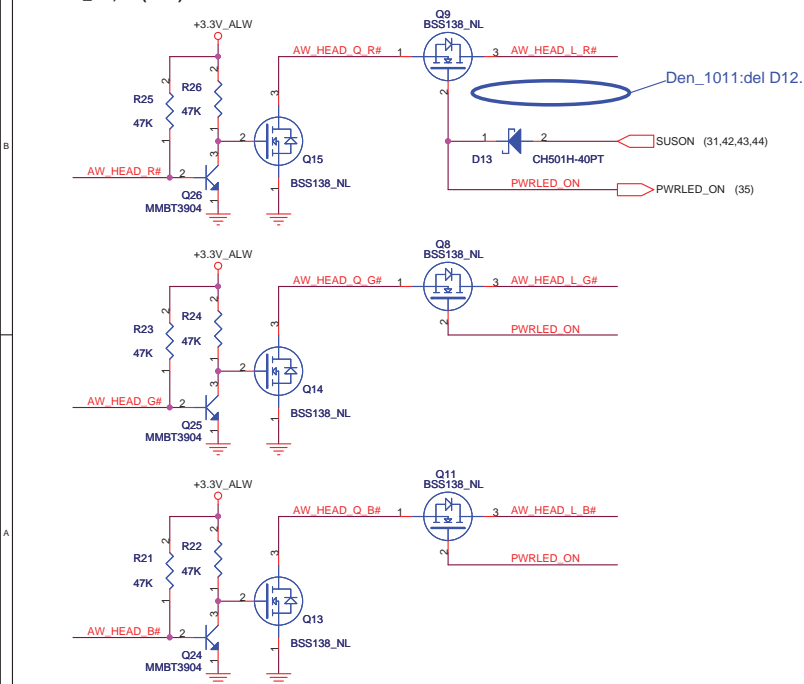


ZONE 1,2,3 --- ELC Controller (LCD Panel, A-Cover)



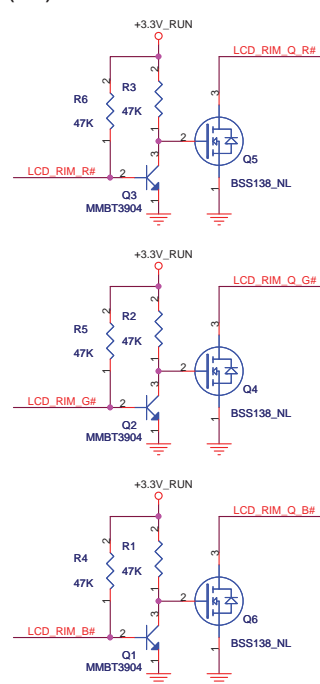
ZONE 1 --- AW Head Buffer (A-Cover, RGB LED*3)

BSS138_NL, ID (max) = 0.22A

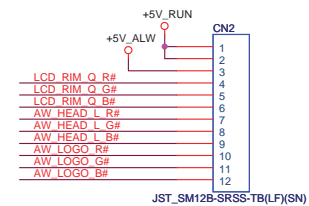


ZONE 2 --- LCD RIM Buffer (A-Cover, RGB LED*4)

BSS138_NL, ID (max) = 0.22A



LED Connector (12 Pins) --- MB to LCD Panel (A-Cover)



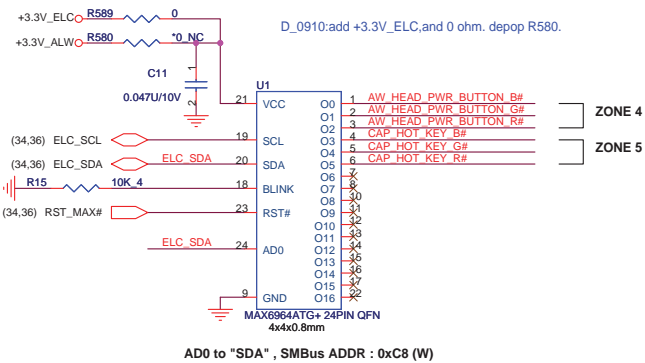
Title ELC TUSB3410VF & ZONE 1-3

Size	Document Number
	MX3

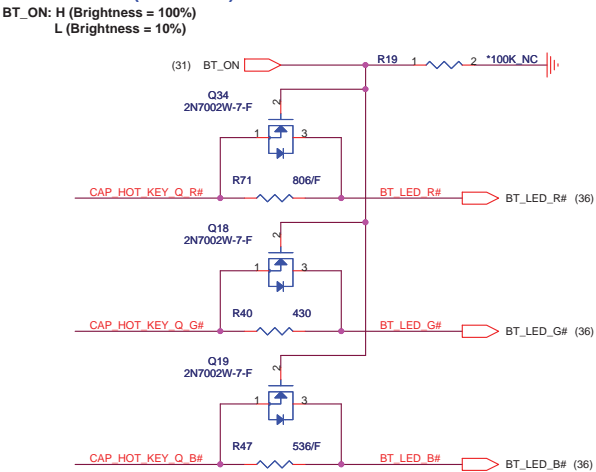
Date: Friday, October 12, 2007

Rev
3

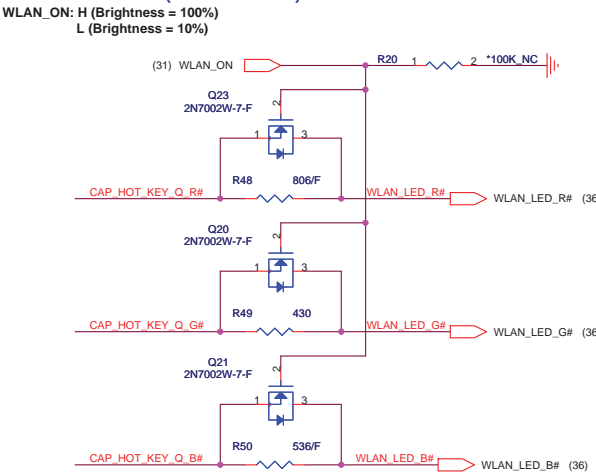
ZONE 4,5 --- ELC Controller (MMB Right/Left Board, C-Cover)



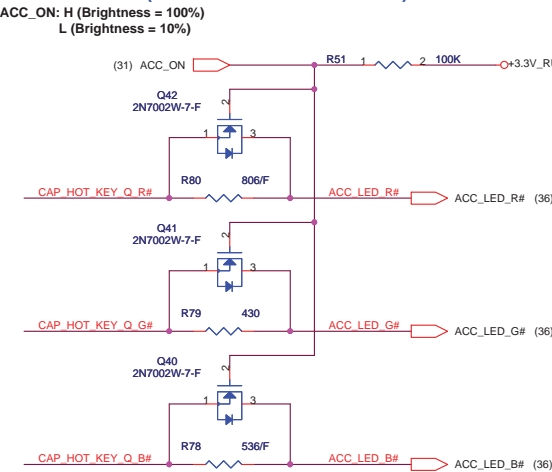
ZONE 5 --- BT (Bluetooth) LED



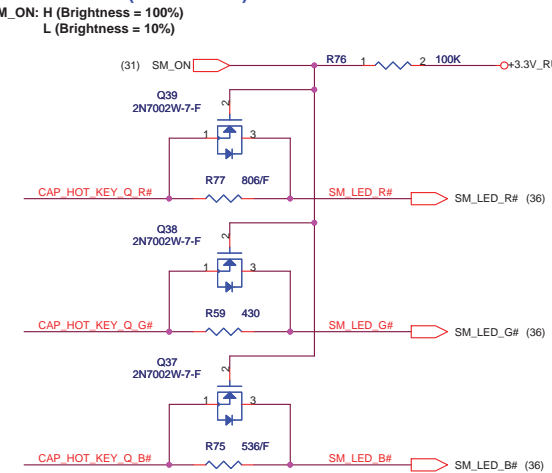
ZONE 5 --- WLAN (Wireless LAN) LED



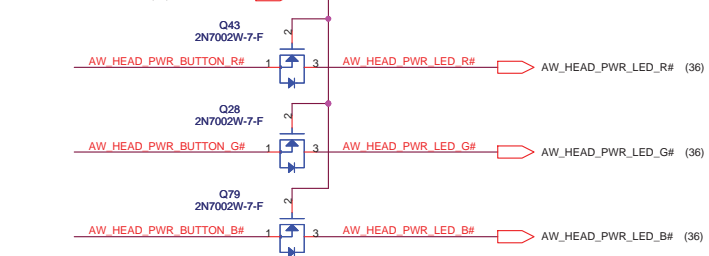
ZONE 5 --- ACC (Alienware command center) LED



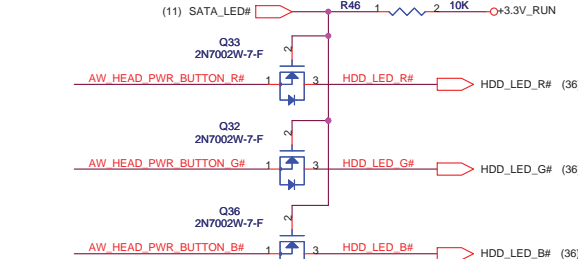
ZONE 5 --- SM (Silent Mode) LED



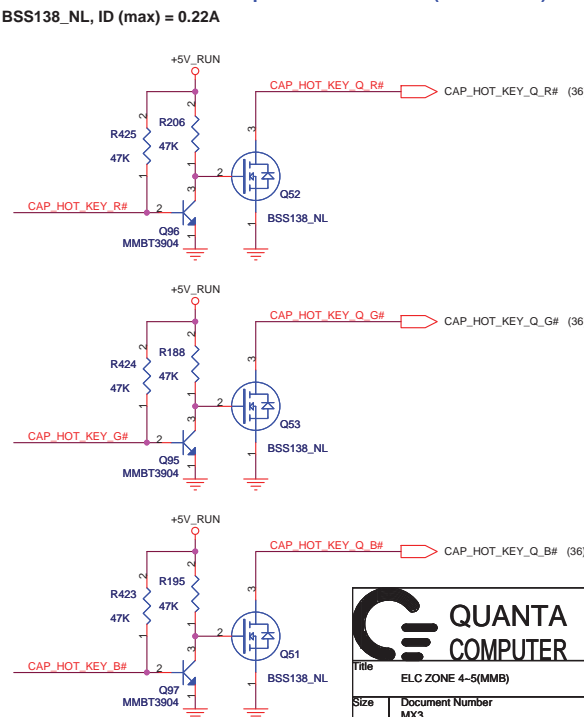
ZONE 4 --- Power Status--AW_Head_RIM (C-Cover, RGB LED*1)



ZONE 4 --- HDD ACT--AW_Head_Eyes (C-Cover, RGB LED*1)



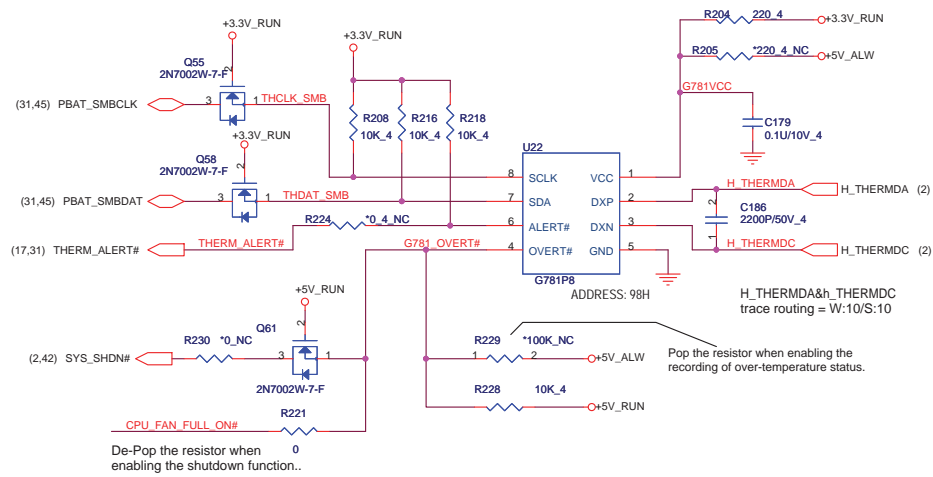
ZONE 5 --- LED Buffer (C-Cover, RGB LED*7)
1.MMB Right -- BT/WLAN/ACC/SM (RGB LED*4)
2.MMB Left -- Caps/Num/Scroll Lock (RGB LED*3)



THERMAL

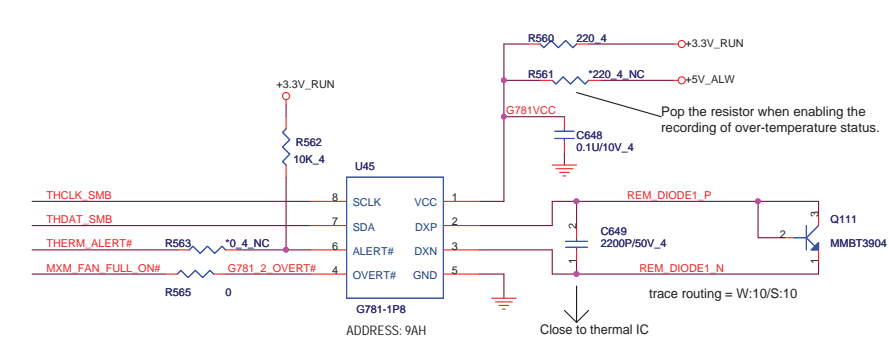
A: FOR CPU TEMP.

B: MB SKIN TEMP (CPU SIDE)



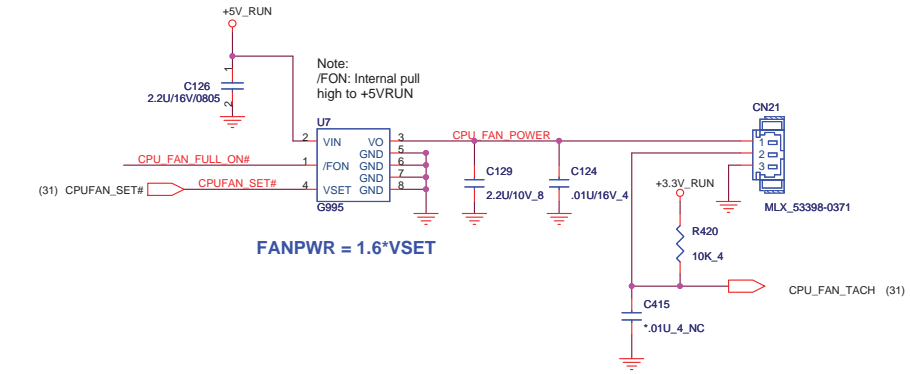
Note: The Over-Temperature flags stay high until cleared by POR, or until the status byte register is read.

C: FOR MXM MODULE TEMP.
D: MB SKIN TEMP (MXM MODULE)

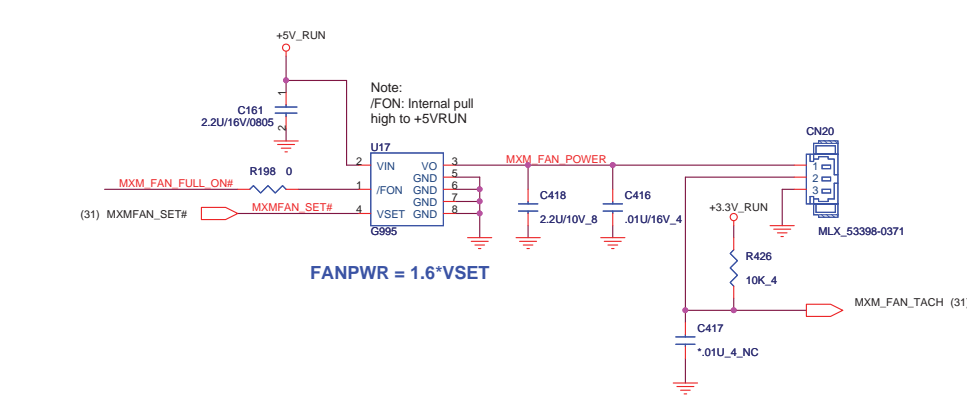


Note: The Over-Temperature flags stay high until cleared by POR, or until the status byte register is read.

CPU FAN

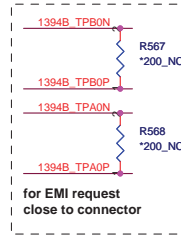
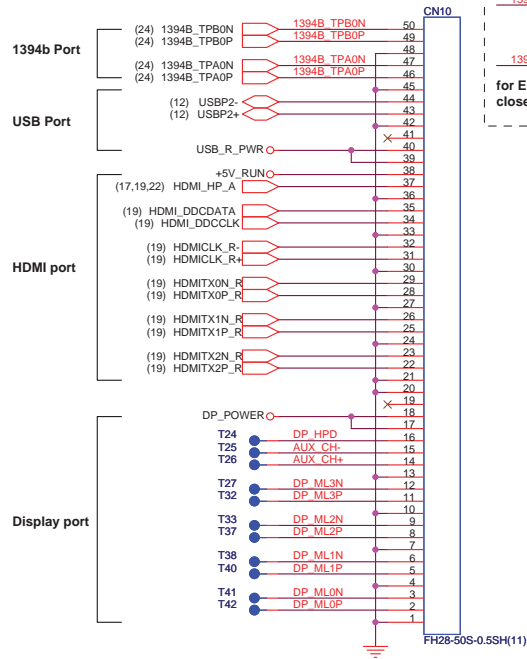
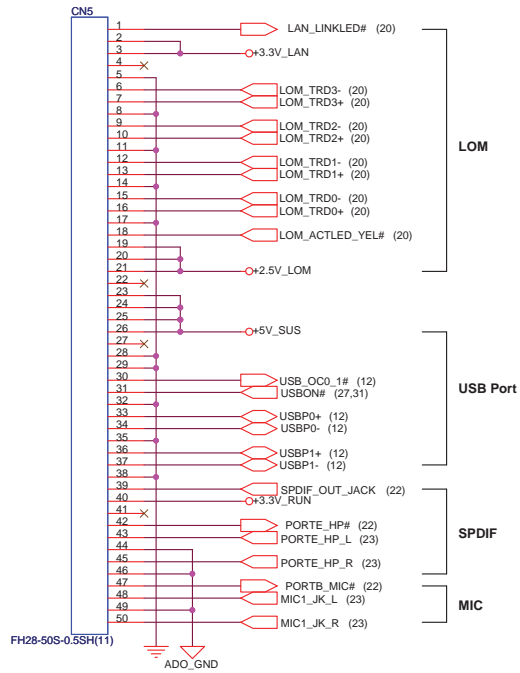


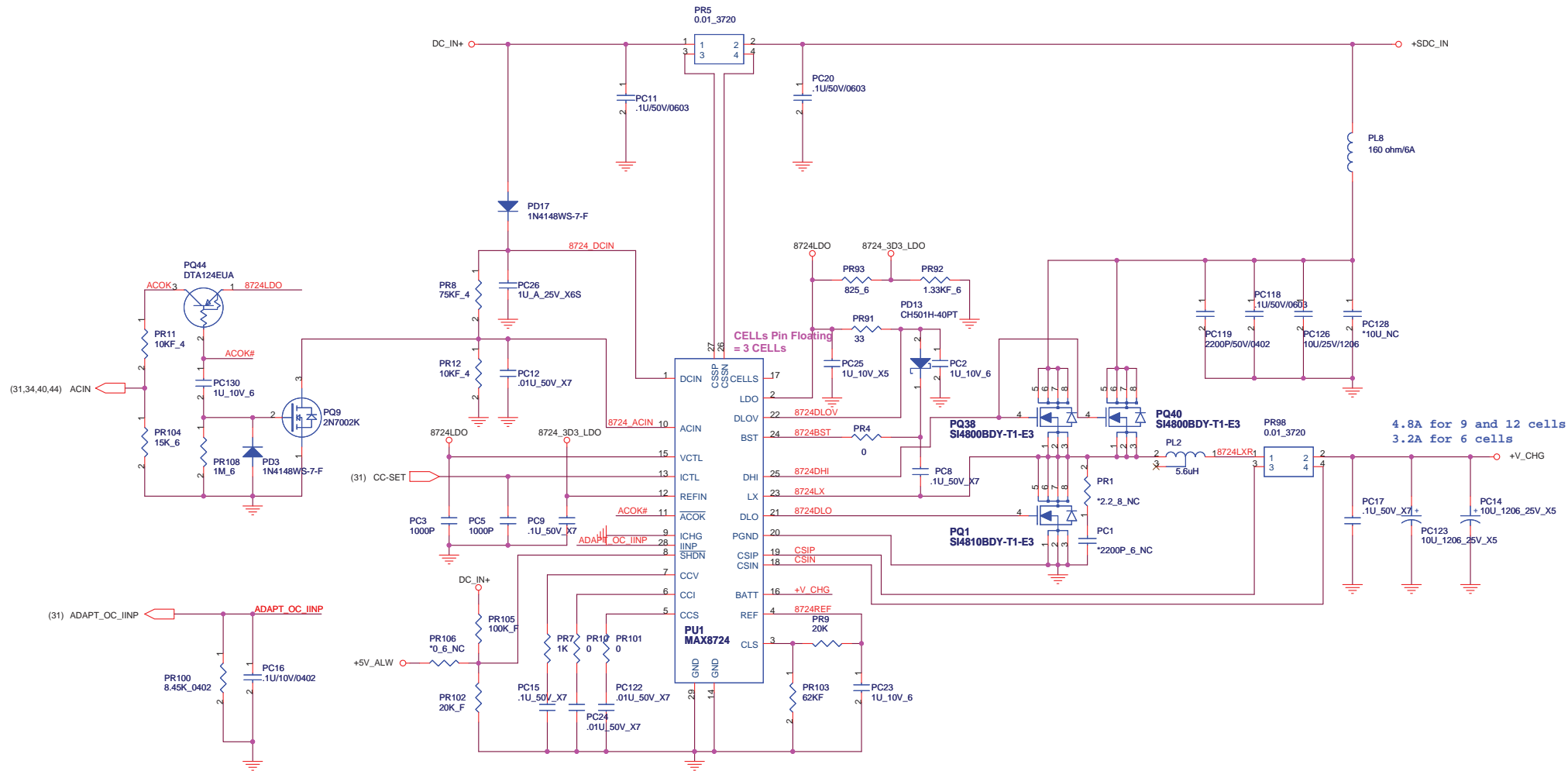
MXM FAN



to AUDIO board connector

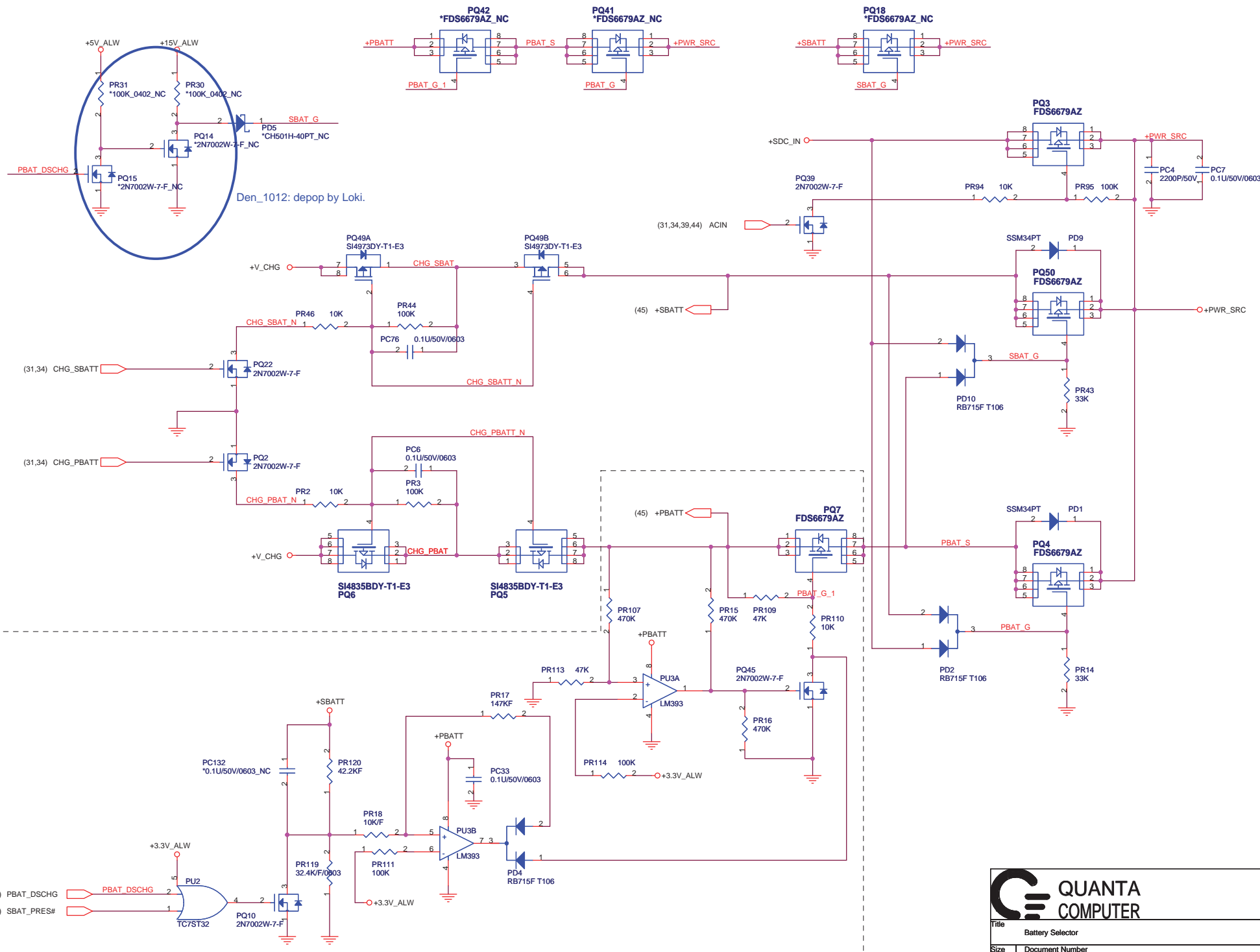
to HDMI board connector

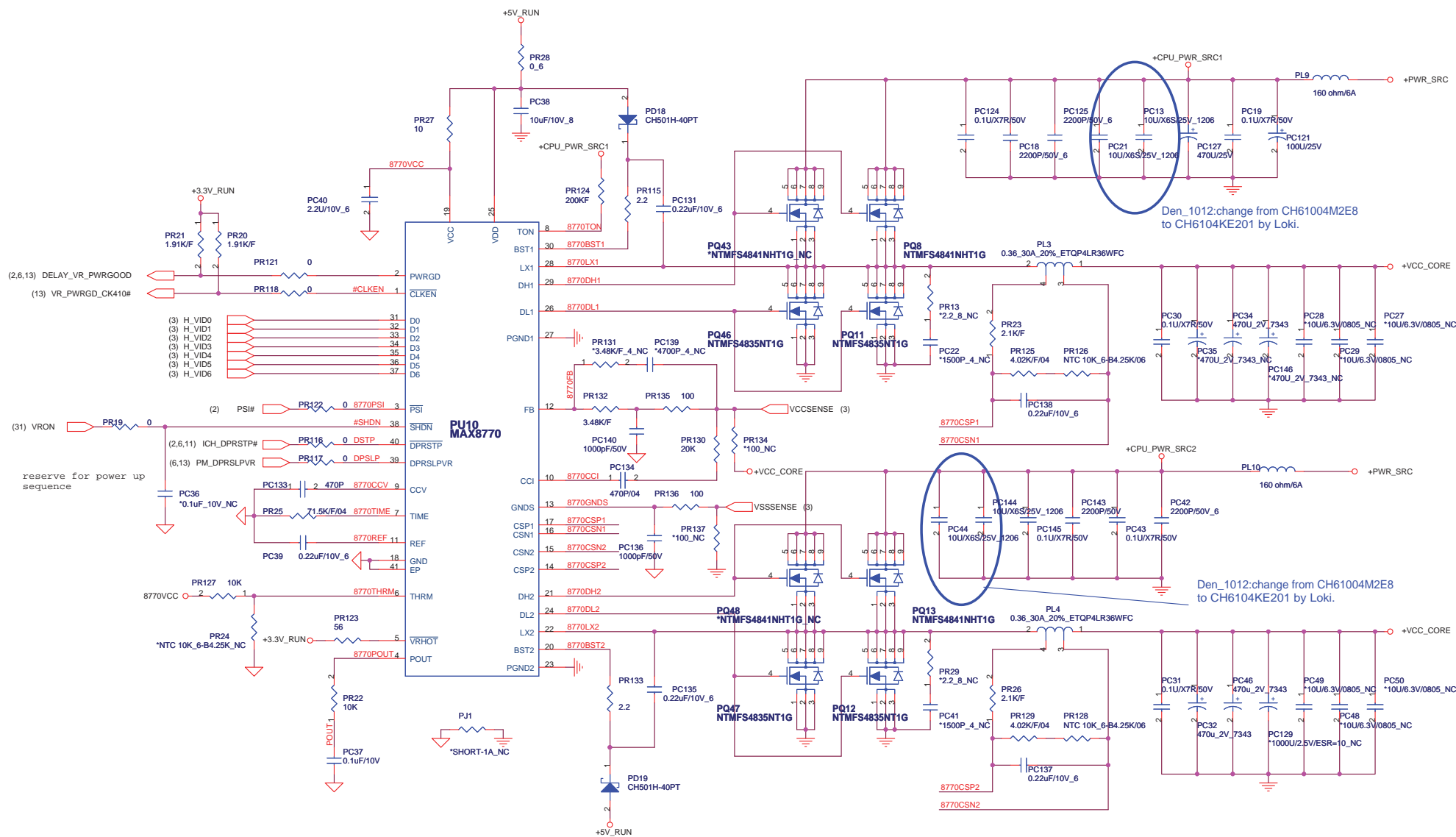


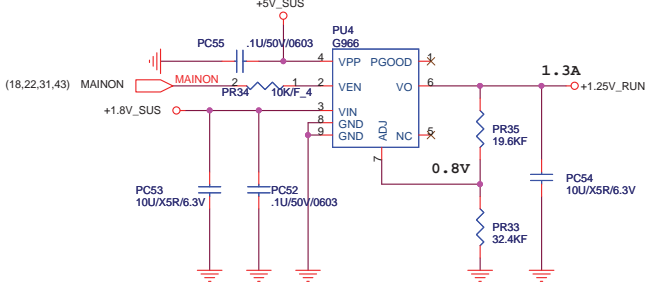
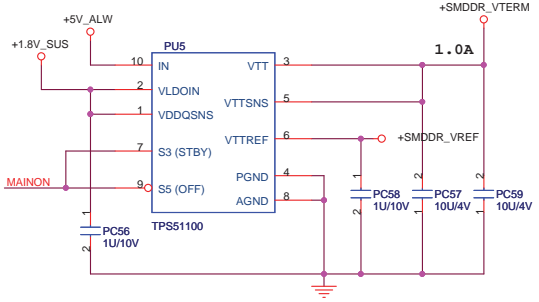
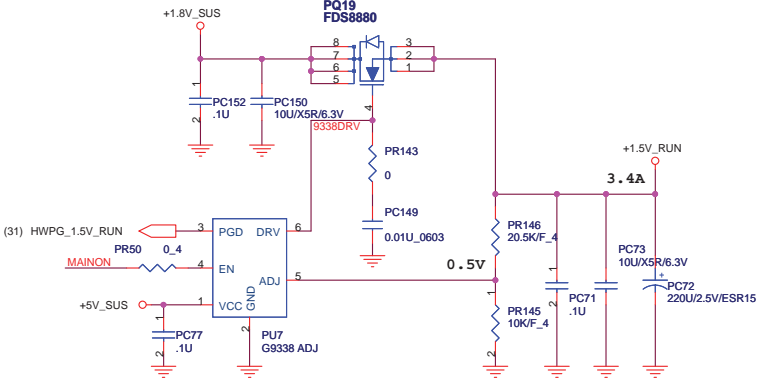
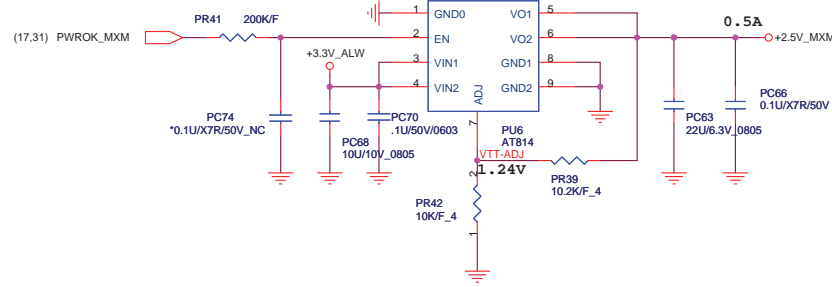
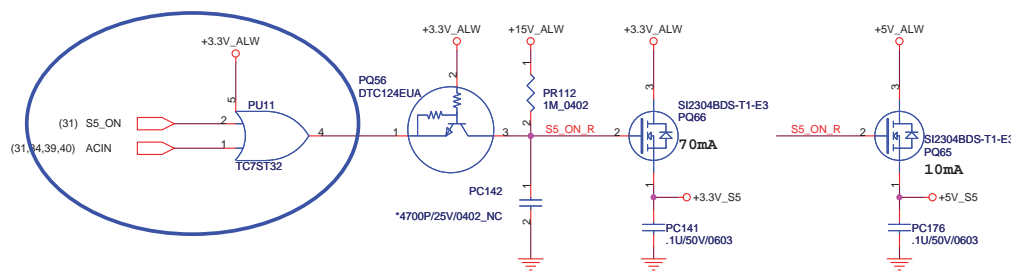
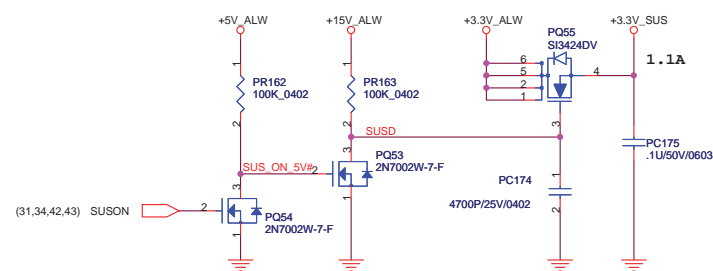
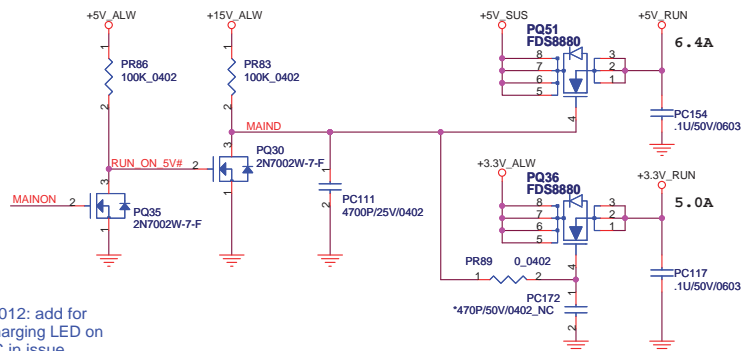


QUANTA
COMPUTER

Title			Charger(MAX8724)
Size	Document Number	Rev	
	MX3	2C	
Date:	Friday, October 12, 2007	Sheet	39 of 53

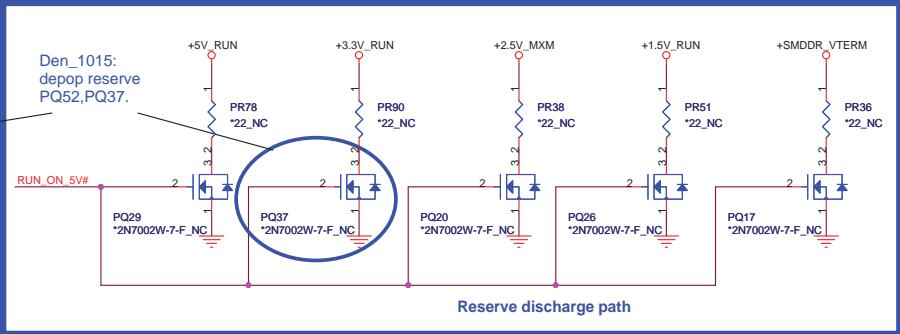
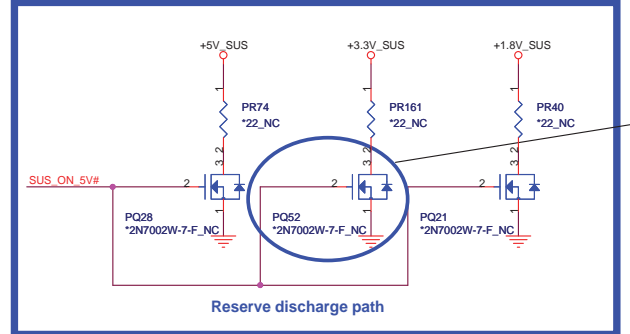


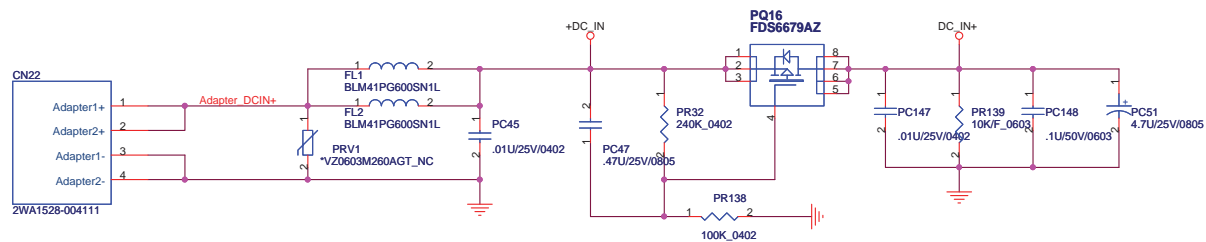
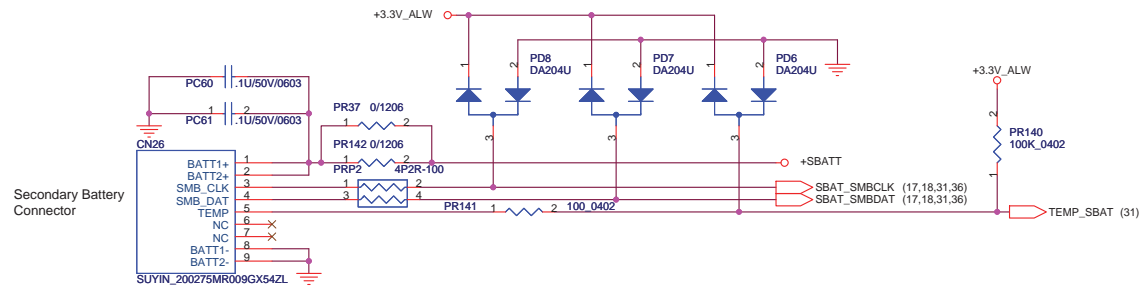
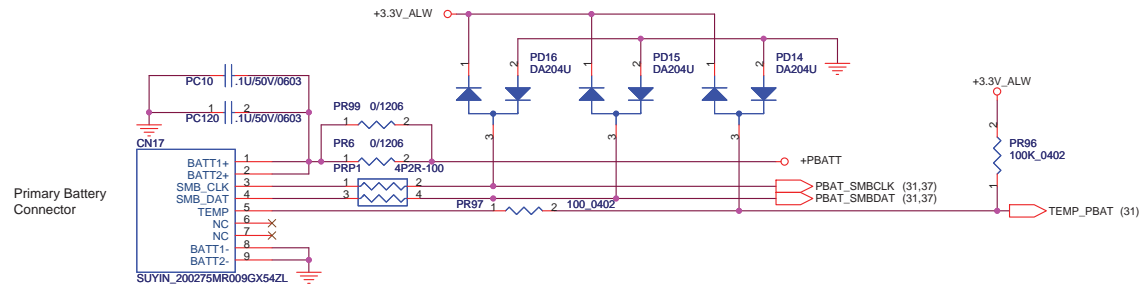




Cancel +1.2V, +5V_S5 and +1.5V_S5

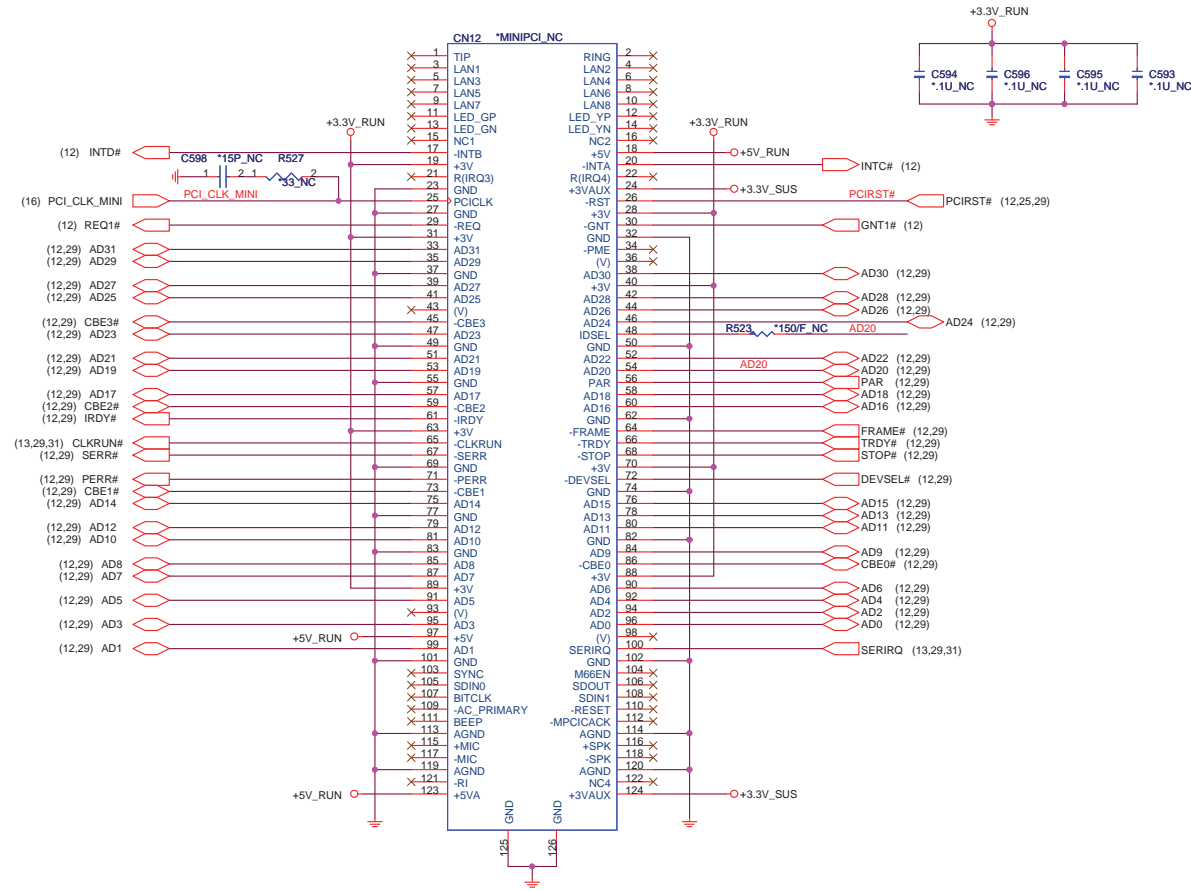
PR33= 32.4K for +1.25_RUN rising up to 1.28V

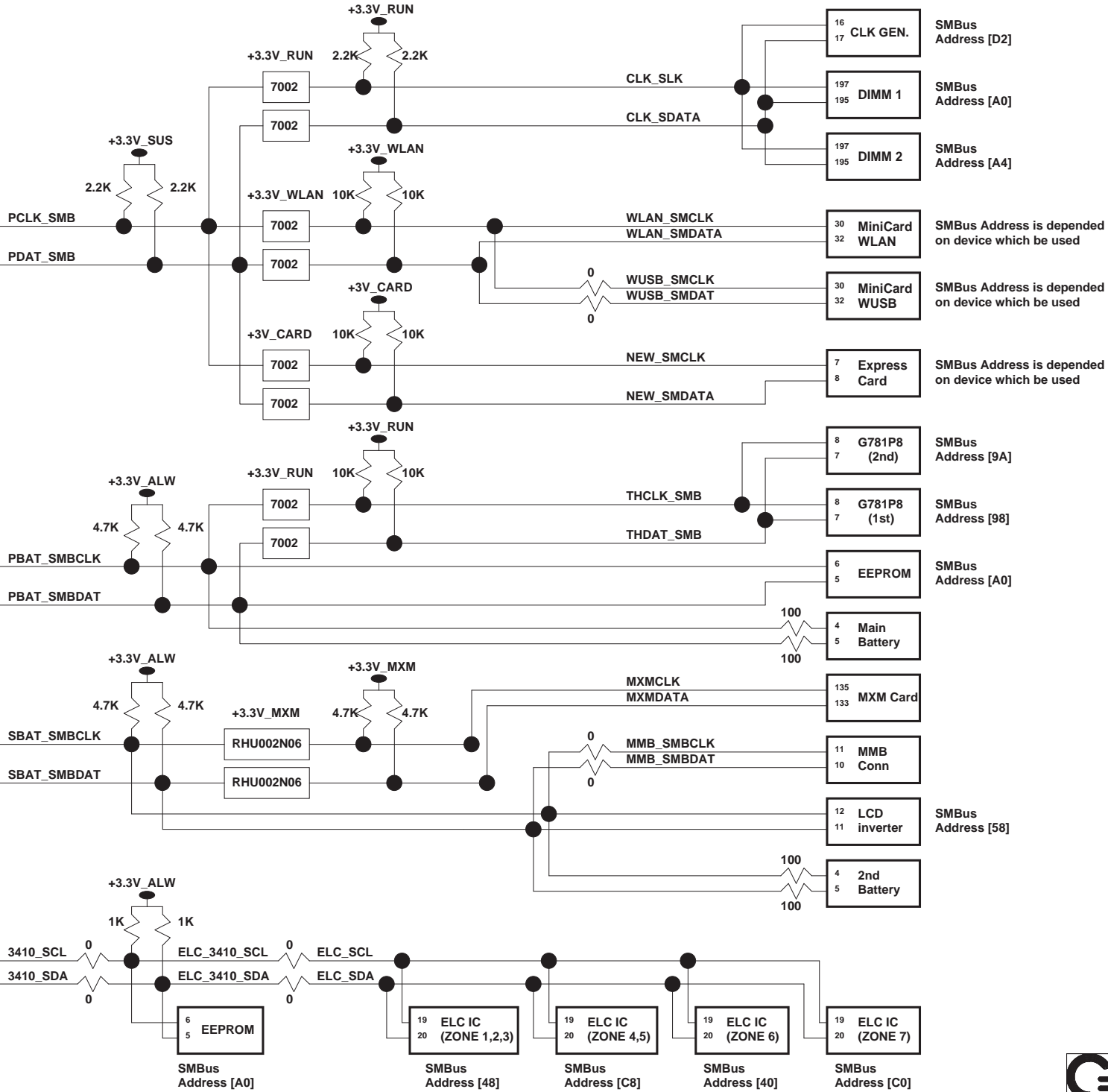
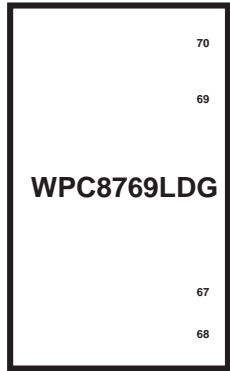




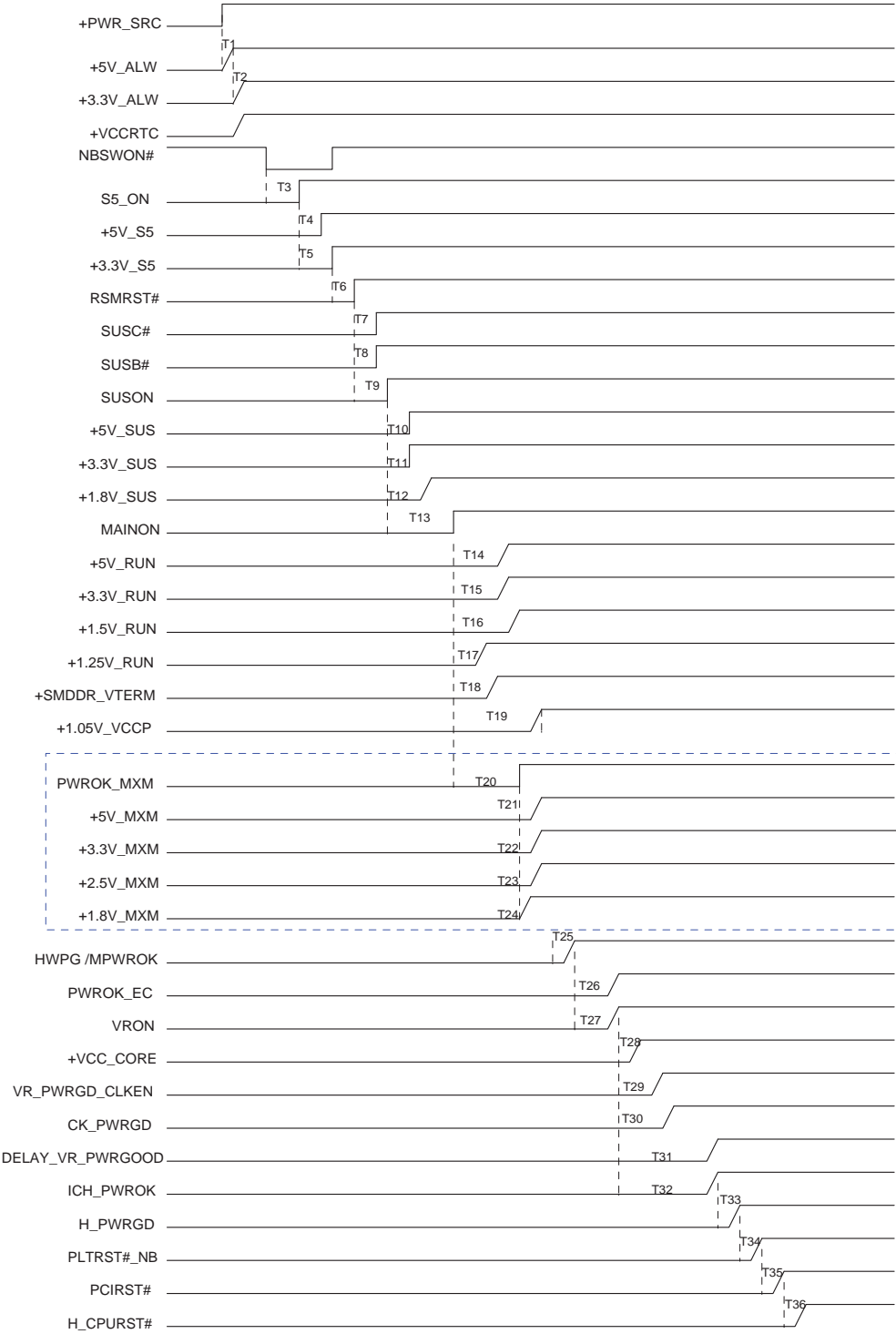
ID Select : AD20
Interrupt Pin : INTC#, INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#

DEBUG PURPOSE ONLY





MX3 Power On Timing



For MXM
Card Power

ITEM	Measure Point		Time
T1	+PWR_SRC	To +5V_ALW	
T2	+5V_ALW	To +3.3V_ALW	
T3	NBSWON#	To S5_ON	
T4	S5_ON	To +5V_S5	
T5	S5_ON	To +3.3V_S5	
T6	+3.3V_S5	To RSMRST#	
T7	RSMRST#	To SUSC#	
T8	RSMRST#	To SUSB#	
T9	RSMRST#	To SUSON	
T10	SUSON	To +5V_SUS	
T11	SUSON	To +3.3V_SUS	
T12	SUSON	To +1.8V_SUS	
T13	SUSON	To MAINON	
T14	MAINON	To +5V_RUN	
T15	MAINON	To +3.3V_RUN	
T16	MAINON	To +1.5V_RUN	
T17	MAINON	To +1.25V_RUN	
T18	MAINON	To +SMDDR_VTERM	
T19	MAINON	To +1.05V_VCCP	
T20	MAINON	To PWROK_MXM	
T21	PWROK_MXM	To +5V_MXM	
T22	PWROK_MXM	To +3.3V_MXM	
T23	PWROK_MXM	To +2.5V_MXM	
T24	PWROK_MXM	To +1.8V_MXM	
T25	+1.05V_VCCP	To HWPG /MPWROK	
T26	HWPG /MPWROK	To PWROK_EC	
T27	HWPG /MPWROK	To VRON	
T28	VRON	To +VCC_CORE	
T29	VRON	To VR_PWRGD_CLKEN	
T30	VRON	To CK_PWRGD	
T31	VRON	To DELAY_VR_PWRGOOD	
T32	VRON	To ICH_PWROK	
T33	ICH_PWROK	To H_PWRGD	
T34	H_PWRGD	To PLTRST#_NB	
T35	PLTRST#_NB	To PCIRST#	
T36	PCIRST#	To H_CPURST#	

